Lattice Semiconductor Corporation
Design Software
Intellectual Property
Development Hardware

Includes
ispLEVER (FPGA/CPLD Devices)
ispLeverCORE IP
PAC-Designer (Power Manager and ispCLOCK Devices)
Development Hardware / Evaluation Boards

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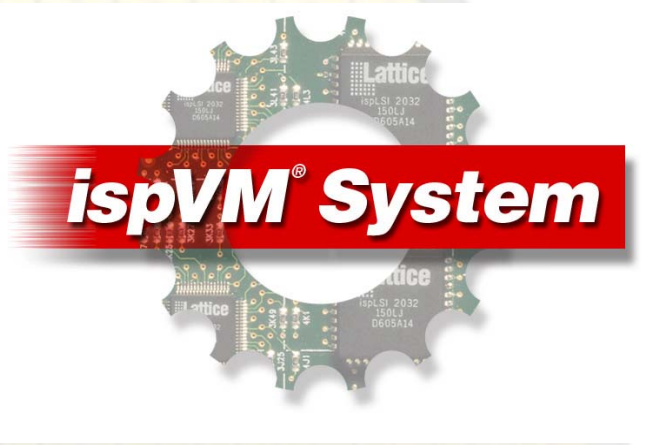
ispLEVER Overview

- **Comprehensive Design Solutions**
- **Easy to Learn**
- **Familiar Flows**
- **All the Tools Required**
- **The Most Choice**
- **Best Performance**
- **Best Value**
- **Best Programming Tools**

“The Simple Machine for Complex Designs”



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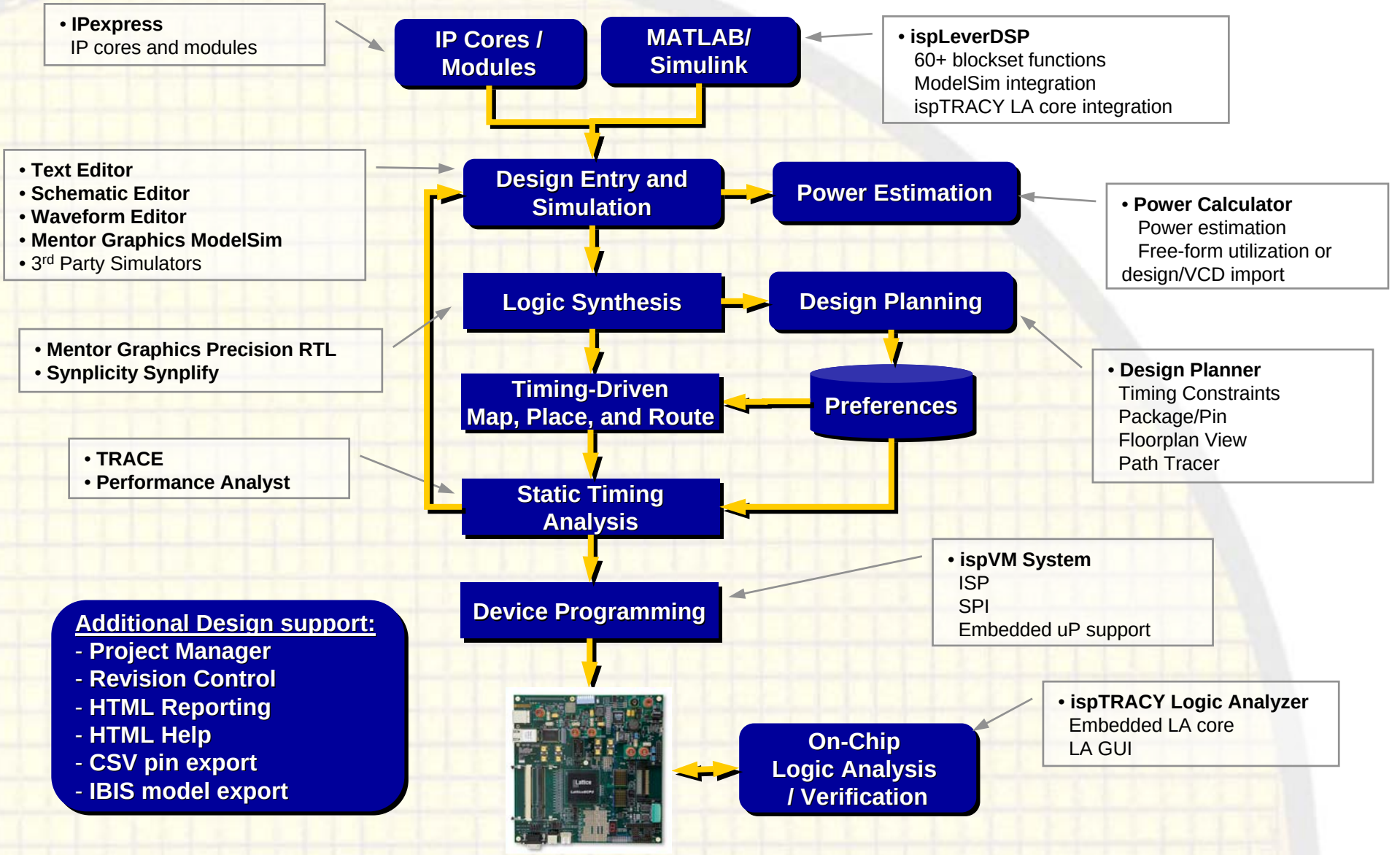
Agenda

- ispLEVER Software Feature Overview
- ispLEVER Versus the Competition
- ispLeverCORE Overview
- PAC-Designer Software Feature Overview
- Development Hardware
- How to Learn More

ispLEVER – Digital Design Tools



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ispLEVER Overview

- Two simple software configurations
  - ispLEVER-Starter is a modular download from Lattice's website After 6 months software is non-operational
  - ispLEVER includes all devices and 3rd party tools (Windows)
- $695 (US) List Price
  - Contact your local Lattice Distributor or visit the Lattice online store for offers
- ispLEVER includes Industry Leading 3rd Party Tools
  - Competitors do NOT
  - Synplify and Precision RTL synthesis
  - ModelSim simulation
- ispLEVER includes MATLAB interface for DSP design
  - Competitors do NOT
- ispLEVER includes logic analyzer for on-chip debug
- ispLEVER Available for Windows, Linux, and UNIX

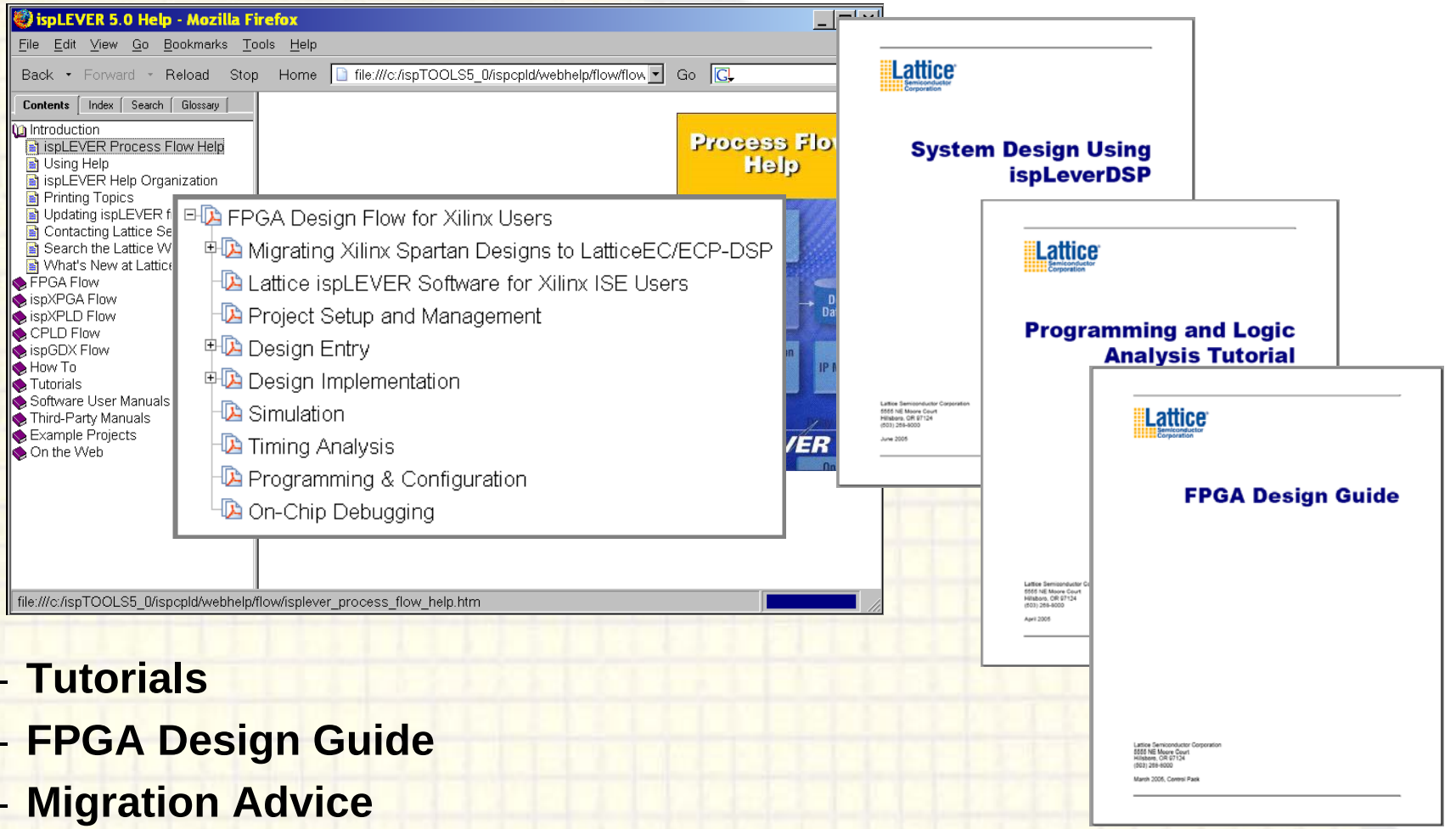
ispLEVER – Design Tools Products

	Part Number	SPLD, GDX/2, CPLD, MachXO	FPGA	FPSC	Included				License Type
					Precision RTL Synthesis	Synplify Synthesis	ModelSim Simulation	Eval Board	
Starter	Downloadable	All	LatticeECP2-50, LatticeECP2-12, All LatticeEC All LatticeECP, LatticeXP3, XP6		Yes	Yes			Node Locked
ispLEVER for Windows	LS-HDL-BASE-PC-N	All	All	All	Yes	Yes	Yes		Node Locked
	LS-EC6-BASE-PC-N	All	All	All	Yes	Yes	Yes	EC6-std	Node Locked
	LS-XP10-BASE-PC-N	All	All	All	Yes	Yes	Yes	XP10-std	Node Locked
	LS-X2280-BASE-PC-N	All	All	All	Yes	Yes	Yes	XO2280-std	Node Locked
ispLEVER for Unix	LS-ADV-WS-F	All	All	All					Floating
ispLEVER for Linux	LS-ADV-LX-F	All	All	All					Floating
Floating License Upgrade for Windows	LS-FLOAT-PC								Floating

ispLEVER: Easy and Quick to Learn

- **Highlights**
  - **FPGA Design Guide**
    - » **Migrating Xilinx and Altera Designs**
    - » **Synthesis Guidelines**
    - » **Timing Closure Advice**
    - » **On-Chip Debug Overview**
  - **Numerous Design Tutorials**
  - **HTML-Based Help Topics with Hyperlinks to Lattice Website**
- **Online Help**
  - **Organized by Lattice Device Category (FPGA, CPLD, etc.) and Design Tool (Power Calculator, Design Planner, etc.)**
  - ***FAST* Search**

Rich Educational Materials



- **Tutorials**
- **FPGA Design Guide**
- **Migration Advice**
- **Hardware Feature *How To* Guides**

It's Easy to Get Started!

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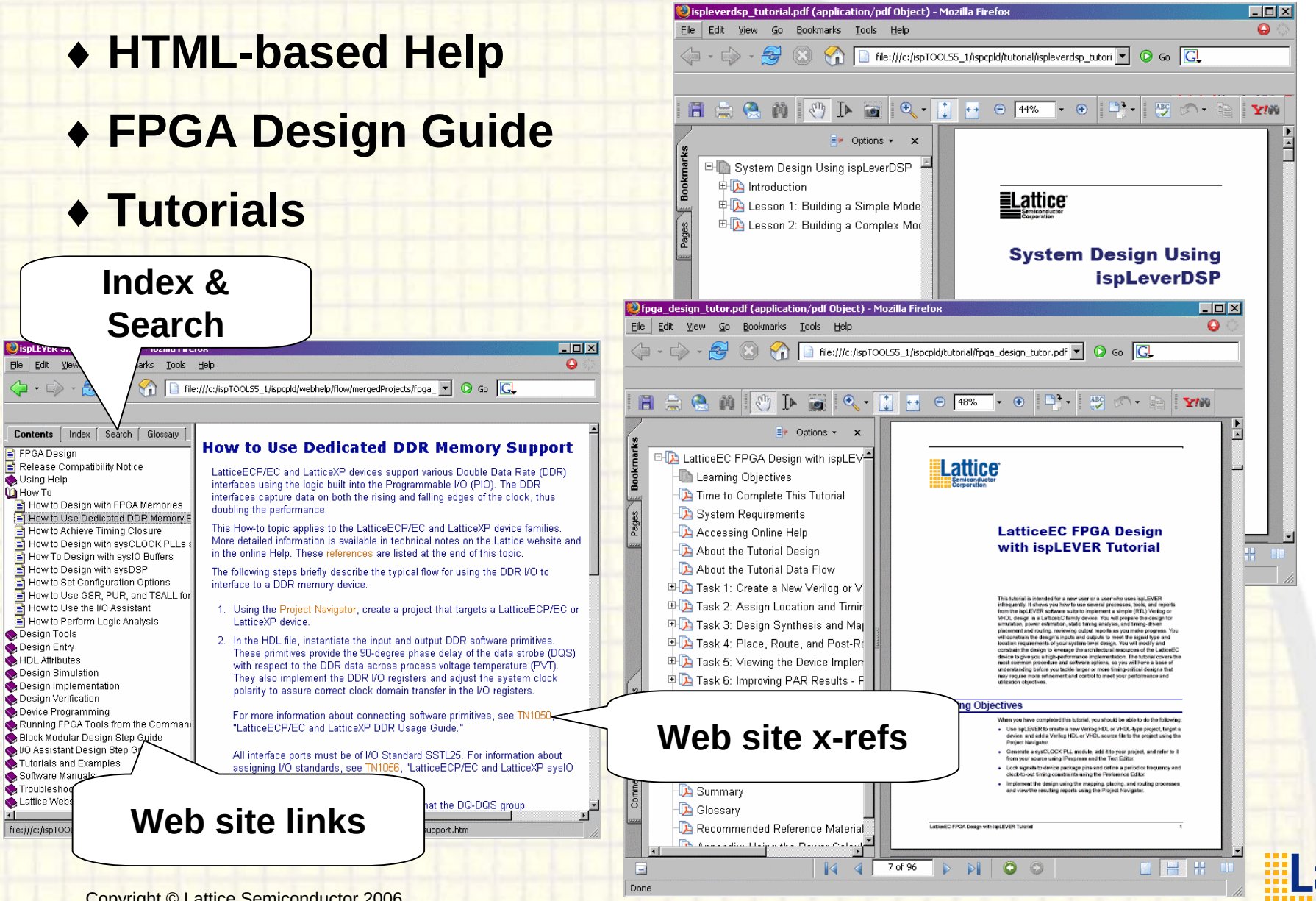
Help, Tutorials, and Design Advice

- HTML-based Help
- FPGA Design Guide
- Tutorials



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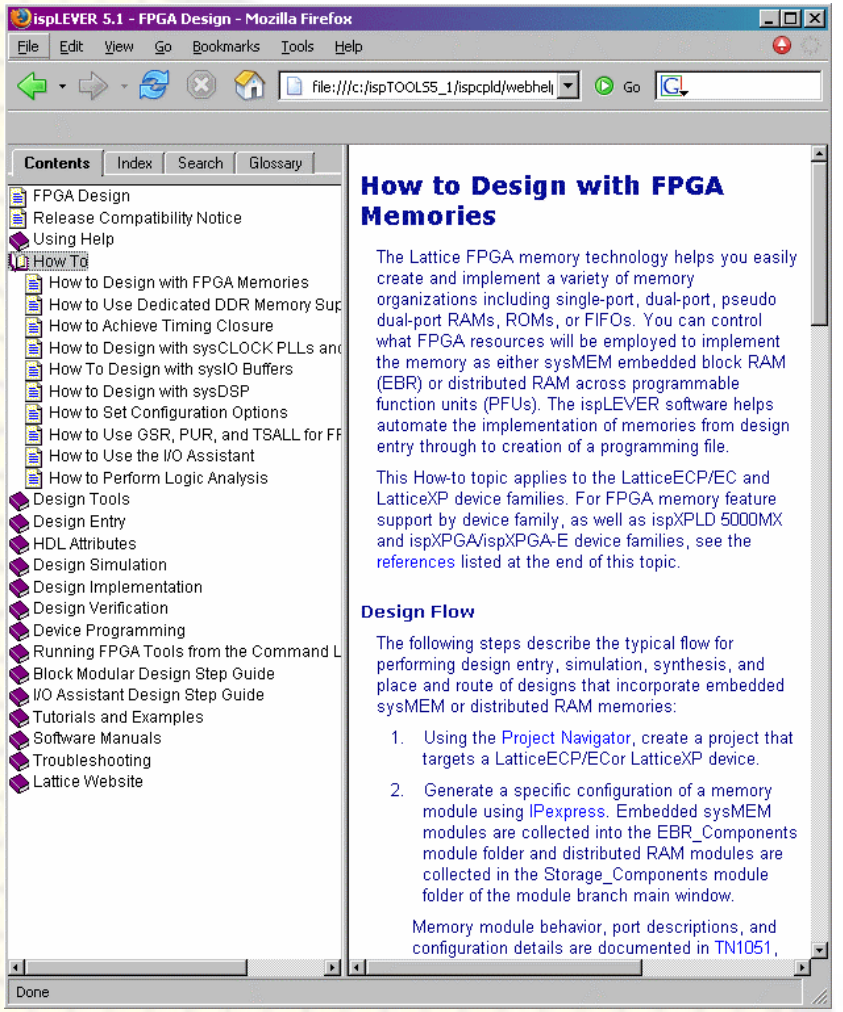
Documentation

- "How To" Help Topics on FPGA functions
  - Memories
  - sysIO Buffers
  - sysCLOCK PLL
  - sysCONFIG
  - sysDSP Blocks
  - DDR
  - More…



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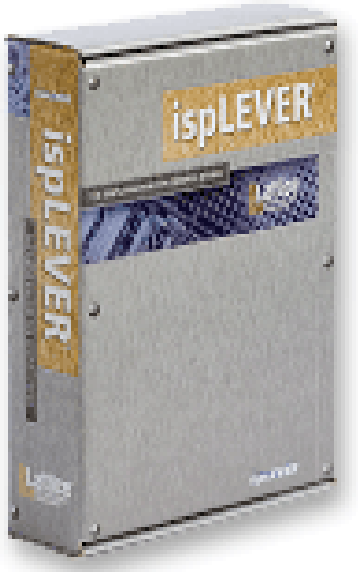
Software Overview

ispLEVER Project Management

- Design Entry
- HDL Synthesis
- Advanced Implementation Tools
- Simulation and Analysis
- Device Programming
- In-system Logic Analysis

Features and Tools



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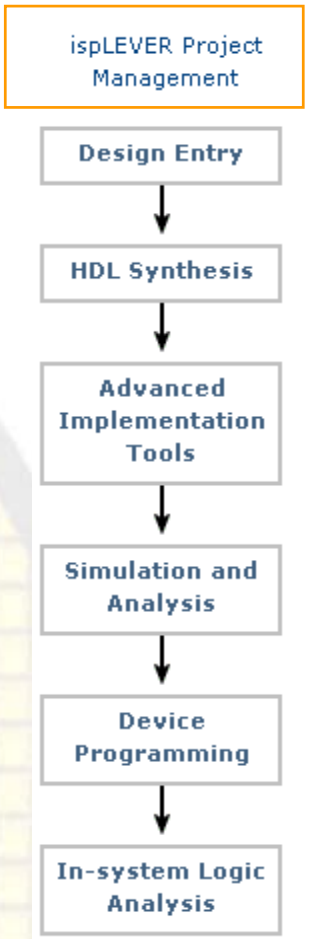
Project Management

- **Project Navigator**
  - Source management and process control
- **Revision Control**
  - Save and restore process state and related files
- **HTML Reporting and Help**
  - Hyperlinked navigation and search of reports and help
- **Tcl/Tk Tools**
  - Record and playback process sequences



Organize Design Files and Processes!

ispLEVER – Project Navigator

Toolbar

Source Window

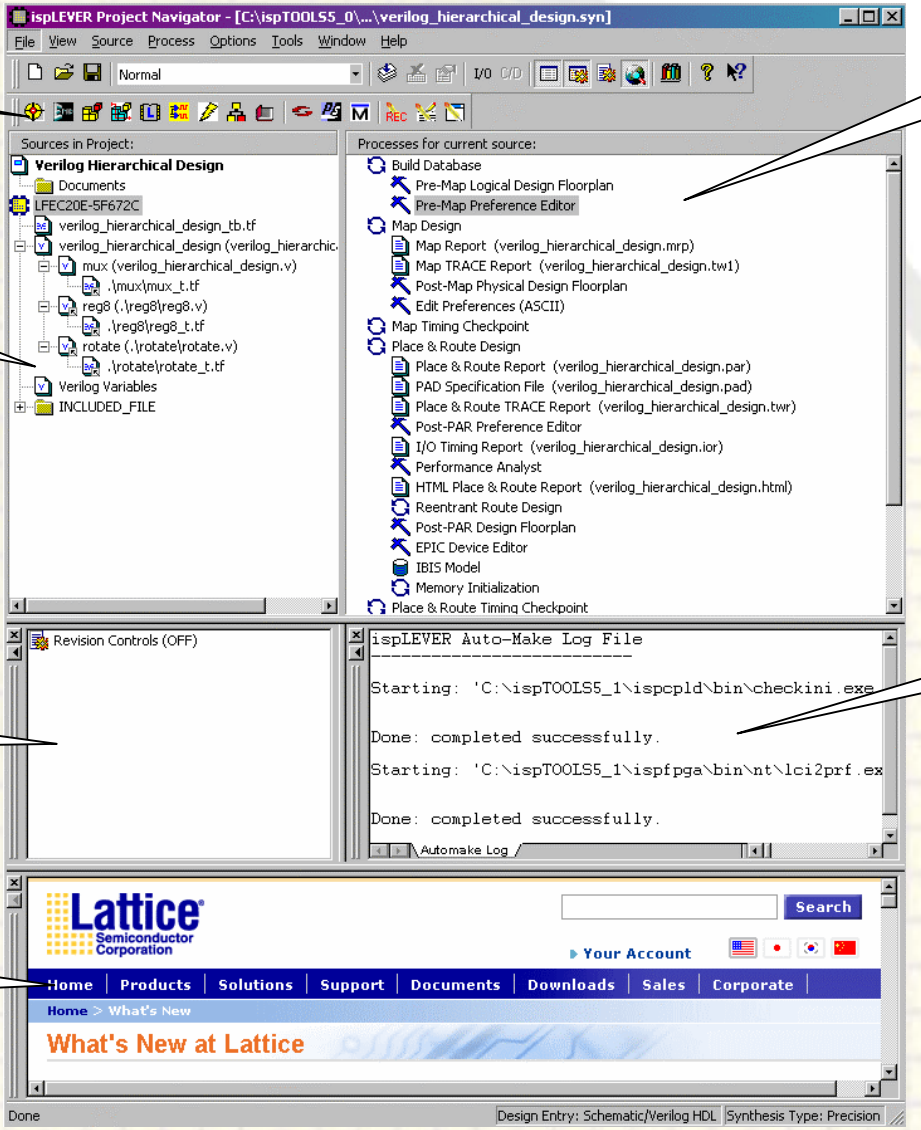
Dockable Windows

Revision Control

What's New?

Process List

Reports



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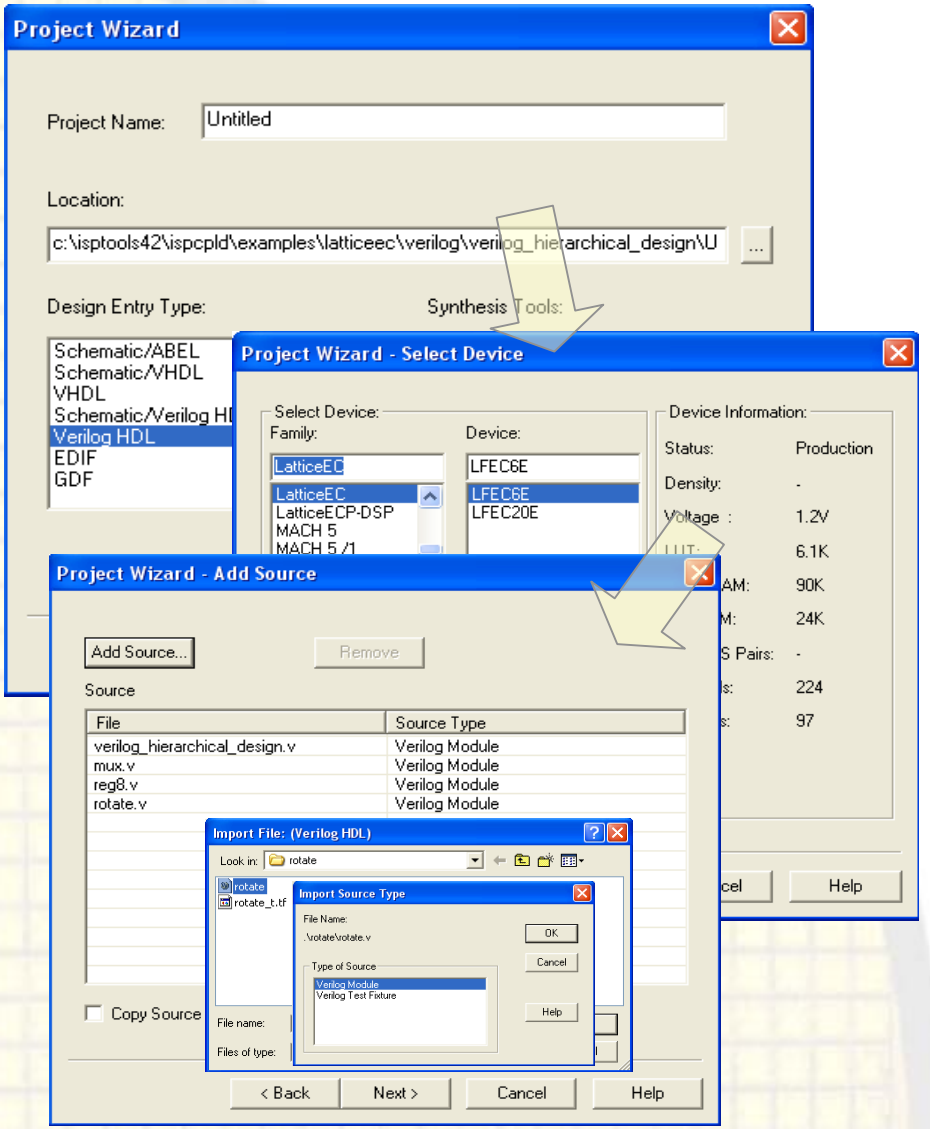
Project Navigator: Project Wizard

- **Design setup <60s**
- **Wizard Choices:**
  - **Name the project**
  - **Select project type**
  - **Select device**
  - **Select source files**
- **When Finished… User Is Designing**



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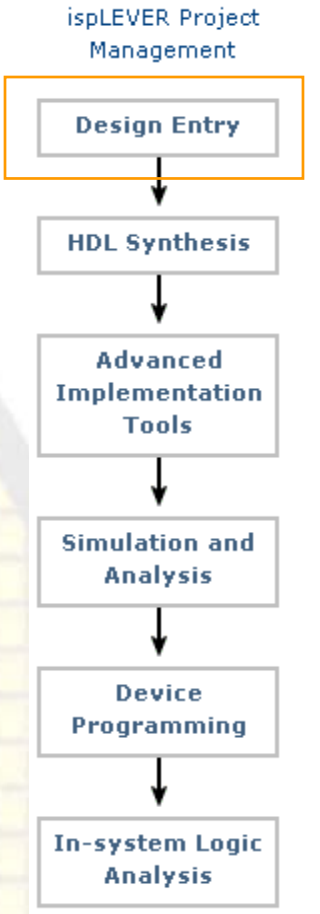
Design Entry Tools

- IPexpress
  - Browse, configure, and generate IP cores
- HDL Text Editor
  - Keyword highlighting for HDL and other native files
- MATLAB/Simulink DSP Blocks
  - DSP-function blocks tailored for Lattice devices
- I/O Assistant method
  - Flow enables early PCB handoff
  - Comprehensive design rule checks
- Block Modular Design method
  - Parallel development of sub-modules
  - Non-invasive incremental design
- Schematic Editor
  - Hierarchical block diagram editor
  - Integrated FPGA libraries
- ABEL for CPLD and SPLD



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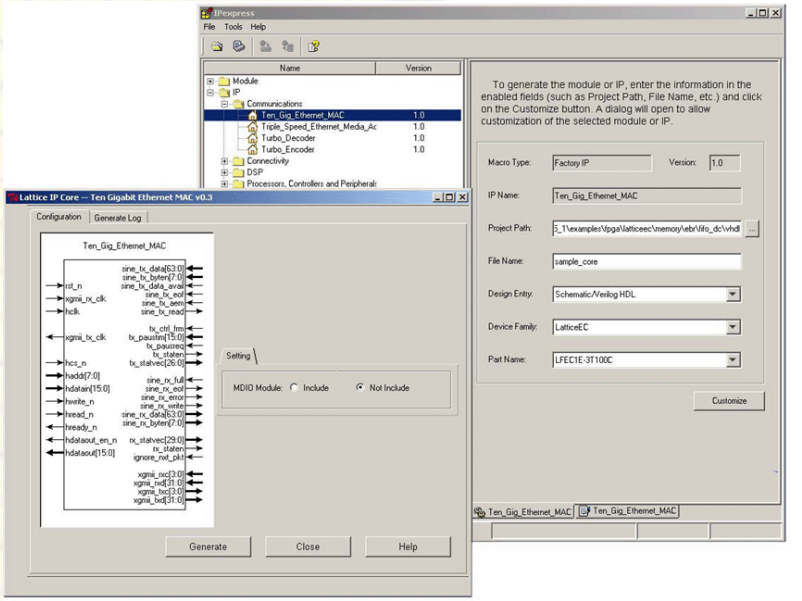
IPexpress

IPexpress
USER CONFIGURABLE

- **Cockpit for Parameterization of Lattice IP Core and Modules**
  - View IP cores available for download
  - Configure and manage IP cores
  - Only device-compatible cores made visible
- **Module Generation**
  - Memories
  - Common digital macro functions
  - sysCLOCK PLL and DLL
  - DDR interfaces
- **Evaluate in Hardware**
  - Includes hardware timeout circuitry
- **Very Easy For Users**
  - No intimate architectural knowledge required



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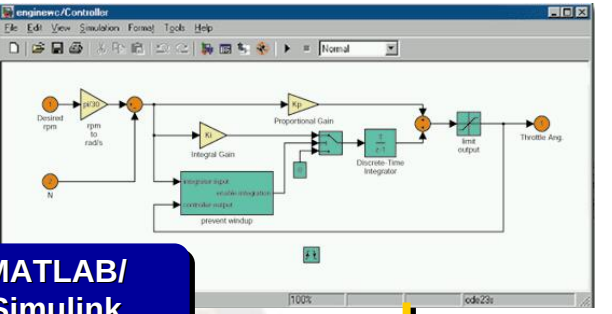
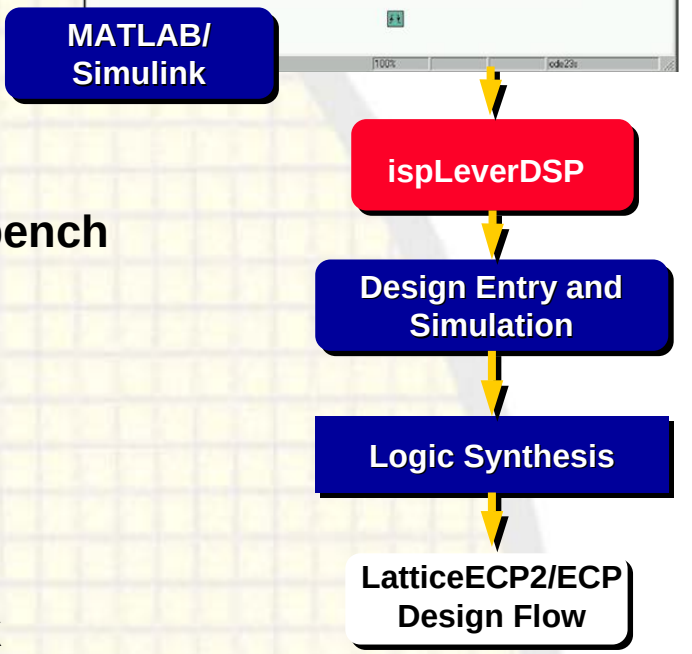
ispLeverDSP MATLAB/Simulink Interface

- **The MathWorks**
  - MATLAB – de-facto standard language for math functions
  - Simulink – graphical design editor for DSP design
  - MathWorks Partner
- **Lattice Simulink Blockset:**
  - Common DSP function blocks
  - Total of 60+ blocks
- **ispLeverDSP**
  - Auto-generates HDL from Simulink design
  - Created HDL testbench matches Simulink testbench
- **Key Features**
  - Subsystem parameterization
  - Propagation of synthesis properties
  - Datatype propagation without simulation
  - Generate special modules using IPexpress
  - Pass parameters through hierarchy in Simulink
  - Tutorials and design examples

Simulink Graphical Editor





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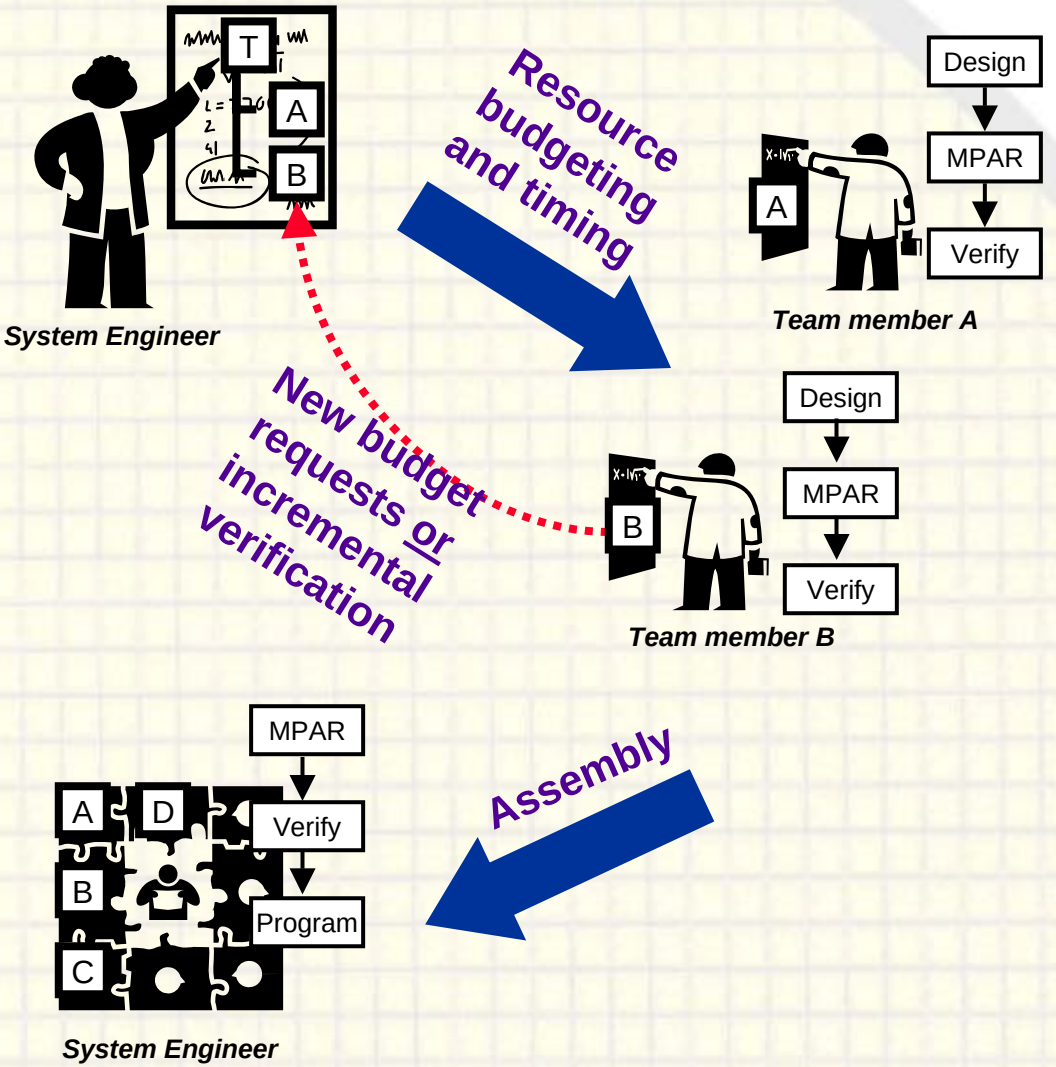
I/O Assistant Method

- ispLEVER Process Flow for I/O Planning
- Supports Early PCB Handoff
  - Select / Check / Lock Pins Before Design is Complete
  - Output to CSV Formatted File
  - Comprehensive Design Rule Checks for I/O Compatibility before Map, Place, and Route
- I/O Module Generation for Complex Interfaces
  - LatticeECP2/ECP/EC/XP
    - DDR_GENERIC
    - DDR_MEM
  - LatticeSC
    - DDR
    - SDR
    - DQS

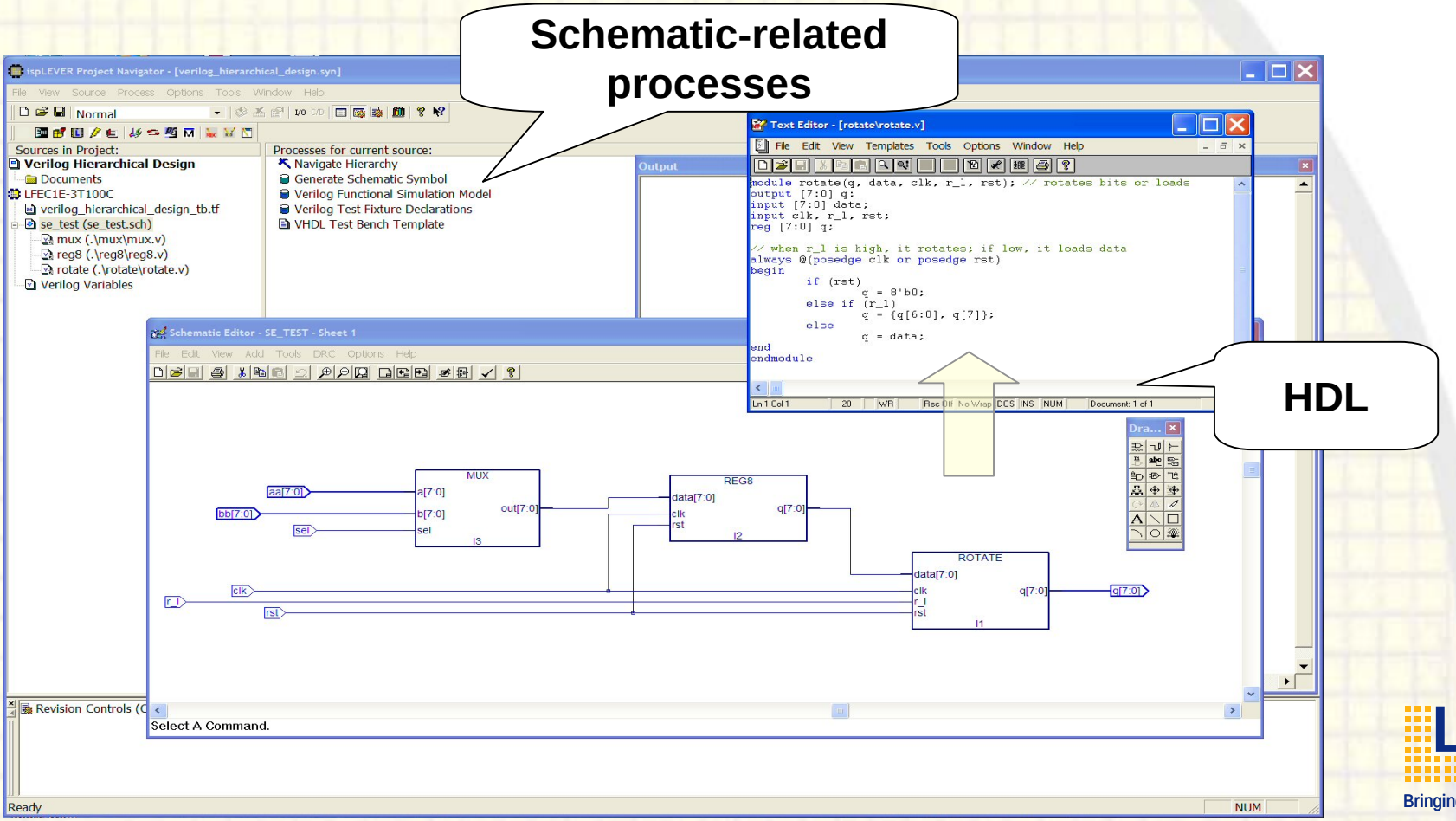
Block Modular Design Method

- ispLEVER Process Flow for Modular Design



ispLEVER Schematic Editor

- Block Diagrams
- Gate-Level FPGA Library
- Import HDL Modules from RTL or IPexpress
- VHDL or Verilog HDL Export



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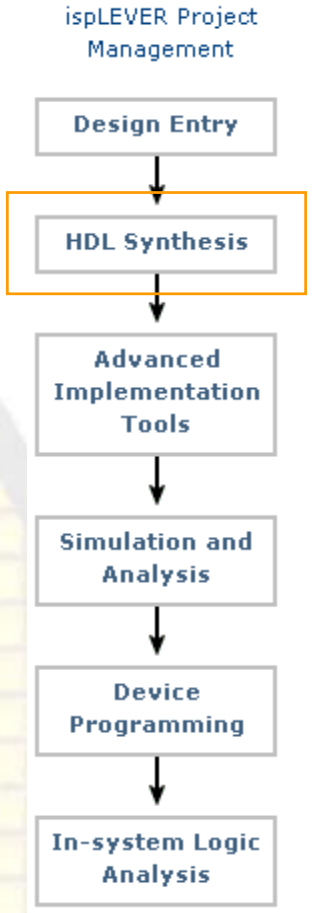
HDL Synthesis

	Precision RTL	Synplify OEM	Synplify Pro
VHDL	✓	✓	✓
Verilog	✓	✓	✓
SystemVerilog	✓		
Constraints Editor	✓	✓	✓
PAR Integration	✓		✓
RTL/Technology View	✓		✓
DSP/RAM/ROM Inferencing	✓	✓	✓



Industry's Best FPGA Synthesis!

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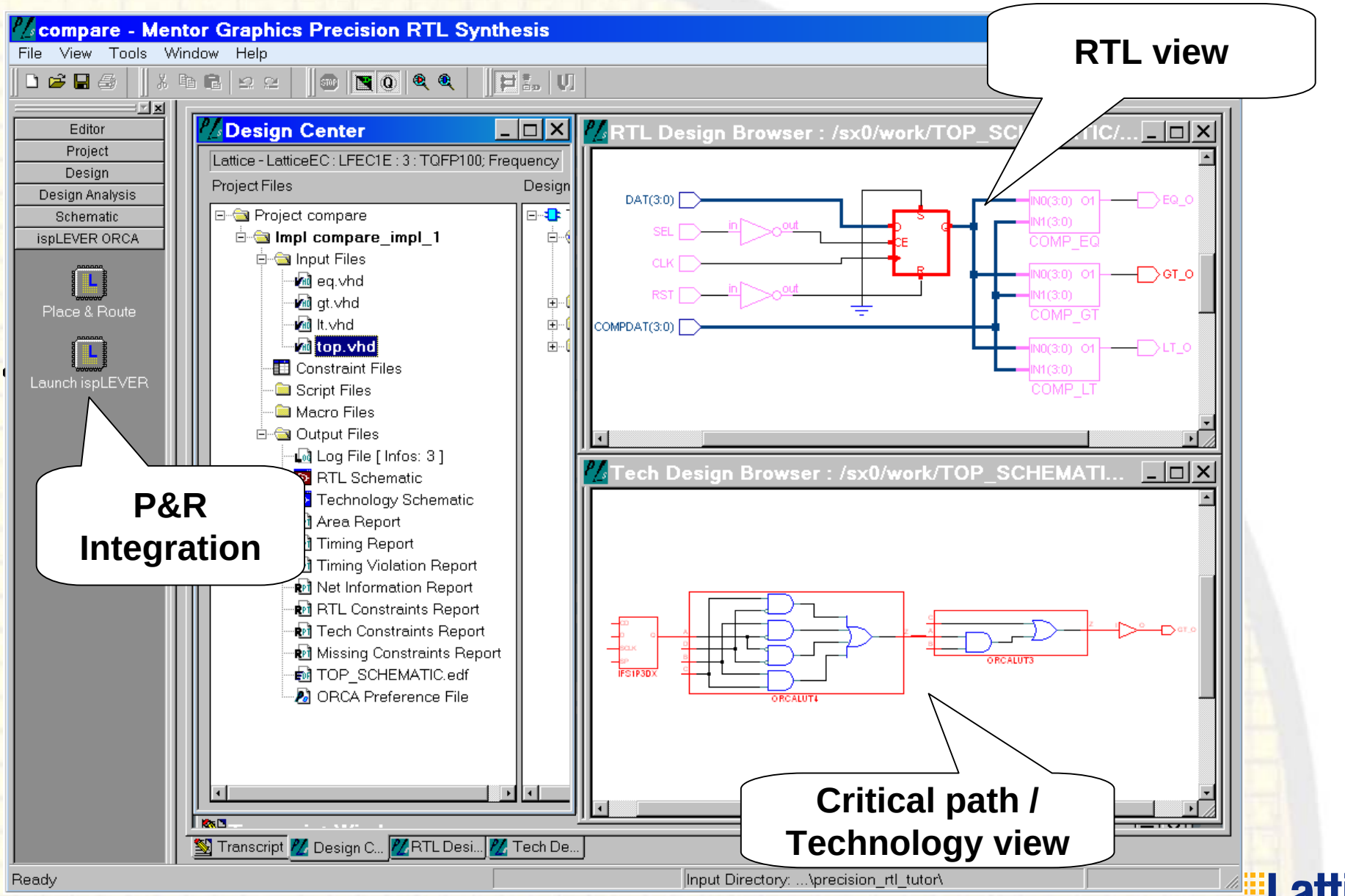
Precision RTL Synthesis for Lattice



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Precision RTL Synthesis

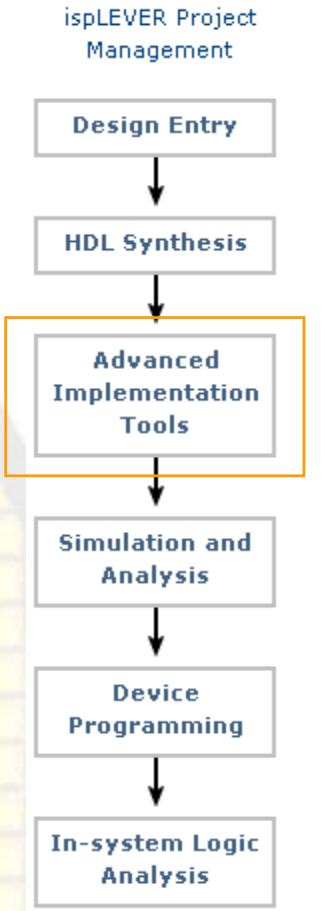
- **Mentor's Latest Synthesis Tool**
  - **Much better f_{MAX} and area utilization than LeoSpec**
  - **Performance very close to Synplicity's Synplify**
  - **More user friendly than LeoSpec**
- **No Differences vs. Mentor's Full Up System**
- **Fully Integrated in ispLEVER**
- **Includes:**
  - **Schematic viewer**
  - **RAM inferencing**
  - **ROM inferencing**
  - **Register retiming**

Synplify for Lattice

- **Synplicity's RTL Synthesis Tool**
- **OEM Version for Lattice Included With ispLEVER**
- **Synplify Pro support now**

Implementation Tools

- **Design Planner**
  - Spreadsheet View
    Excel-like UI to define timing and location Preferences
  - Package View
    Ideal for I/O planning and PCB documentation
  - Floorplan View
    View placement, critical paths, congestion, and groups
  - Path Tracer
    Highlight critical paths
  - Pin CSV Export
- **EPIC Device Editor**
  - Powerful device database editor for ECOs
- **Place & Route**
  - Timing-driven map, place, and route
  - Easy to configure, GUI or command-line driven



Easy to Control and Optimize!

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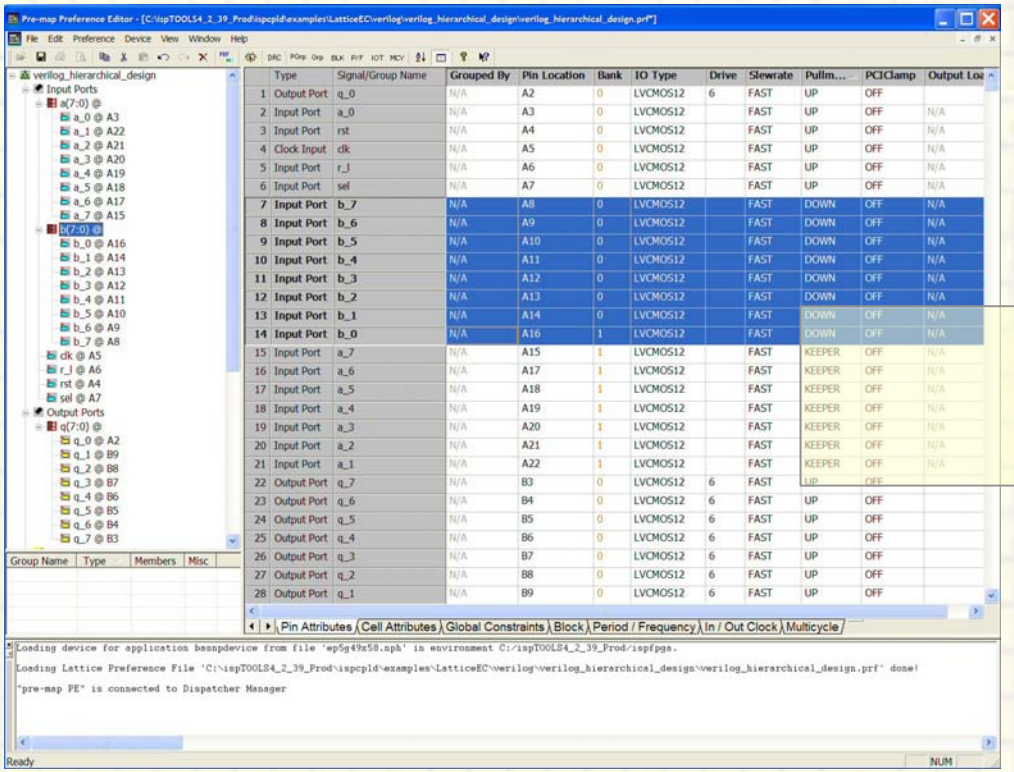
Timing Closure Design Flow

- **Timing Closure Tools Aid In Tuning Design Performance**
  1. **Set Controls To Achieve Timing Goals**
     - » **HDL Source**
     - » **ispLEVER Preferences**
     - » **Floorplan**
     - » **MPAR**
     - » **Static timing analysis**
  2. **Analyze Critical Paths**
  3. **Modify Constraints and Options**
  4. **Iterate As Necessary**

ispLEVER Preference Language

- The Nexus Between Design and Performance
- Flexible ASCII Language for Timing-Driven MPAR and STA
- Graphical Spreadsheet-Like UI Entry Easy
  - Assign Globals, Period/Frequency, I/O Timing, Timing Exceptions




```
FREQUENCY NET "pll_nclk" 133.000000 MHz ;
FREQUENCY NET "pll_mclk" 133.000000 MHz ;
FREQUENCY NET "clk_c" 133.000000 MHz ;
FREQUENCY PORT "clk" 133.000000 MHz ;
DEFINE PORT GROUP "group_dq" "ddr_dq_0"
"ddr_dq_1"
"ddr_dq_2"
"ddr_dq_3"
"ddr_dq_4"
"ddr_dq_5"
"ddr_dq_6"
"ddr_dq_7" ;
CLOCK_TO_OUT GROUP "group_dq" 10.000000 ns CLKPORT "clk" ;
PROHIBIT SITE "EBR_R19C10" ;
PROHIBIT SITE "EBR_R19C8" ;
PROHIBIT SITE "EBR_R19C6"
```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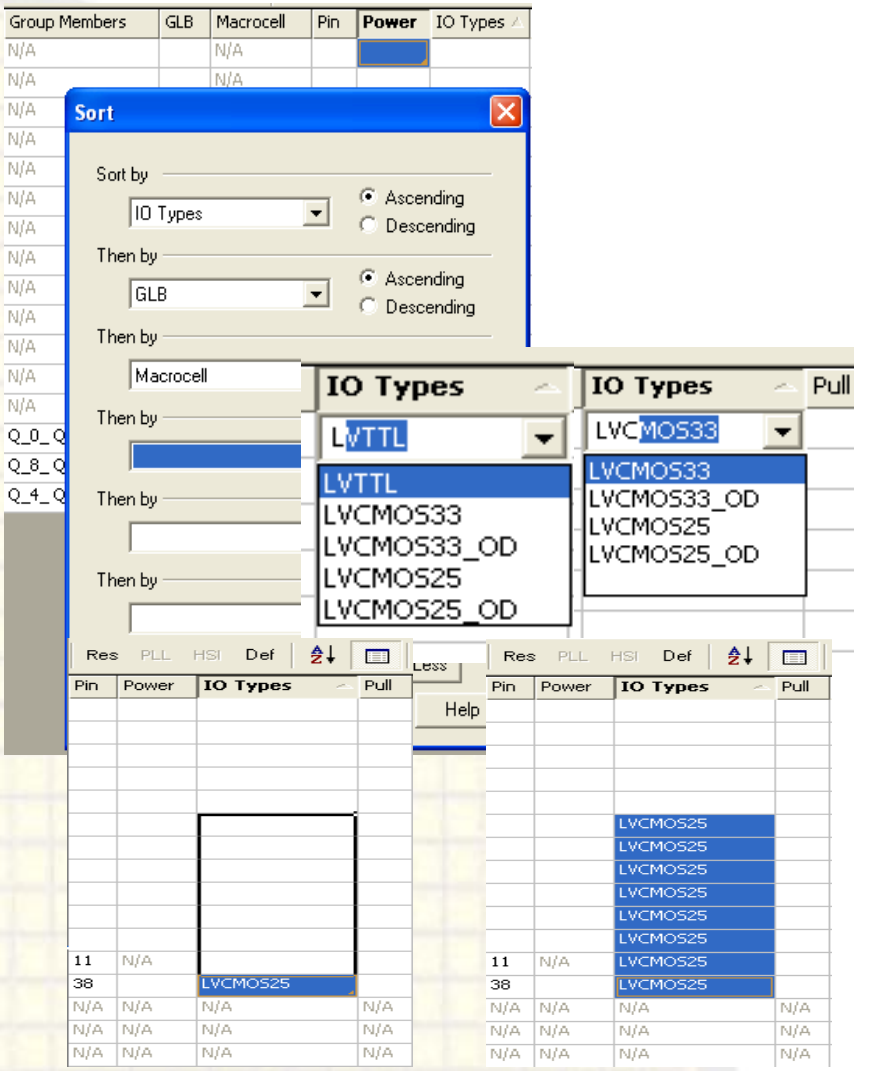
Design Planner: Spreadsheet View

- **Define**
  - I/O Types
  - Pin Assignments
  - Power Options
  - Signal Groups
  - Timing Objectives
  - Multi-Cycle and False Paths
- **Excel-Like Features**
  - Sorting and Pin Type Filters
  - Context Sensitive Menus
  - Fill Up/Down Editing
- **CSV export**
  - ASCII Data Reports
  - 3rd Party Schematic Symbols



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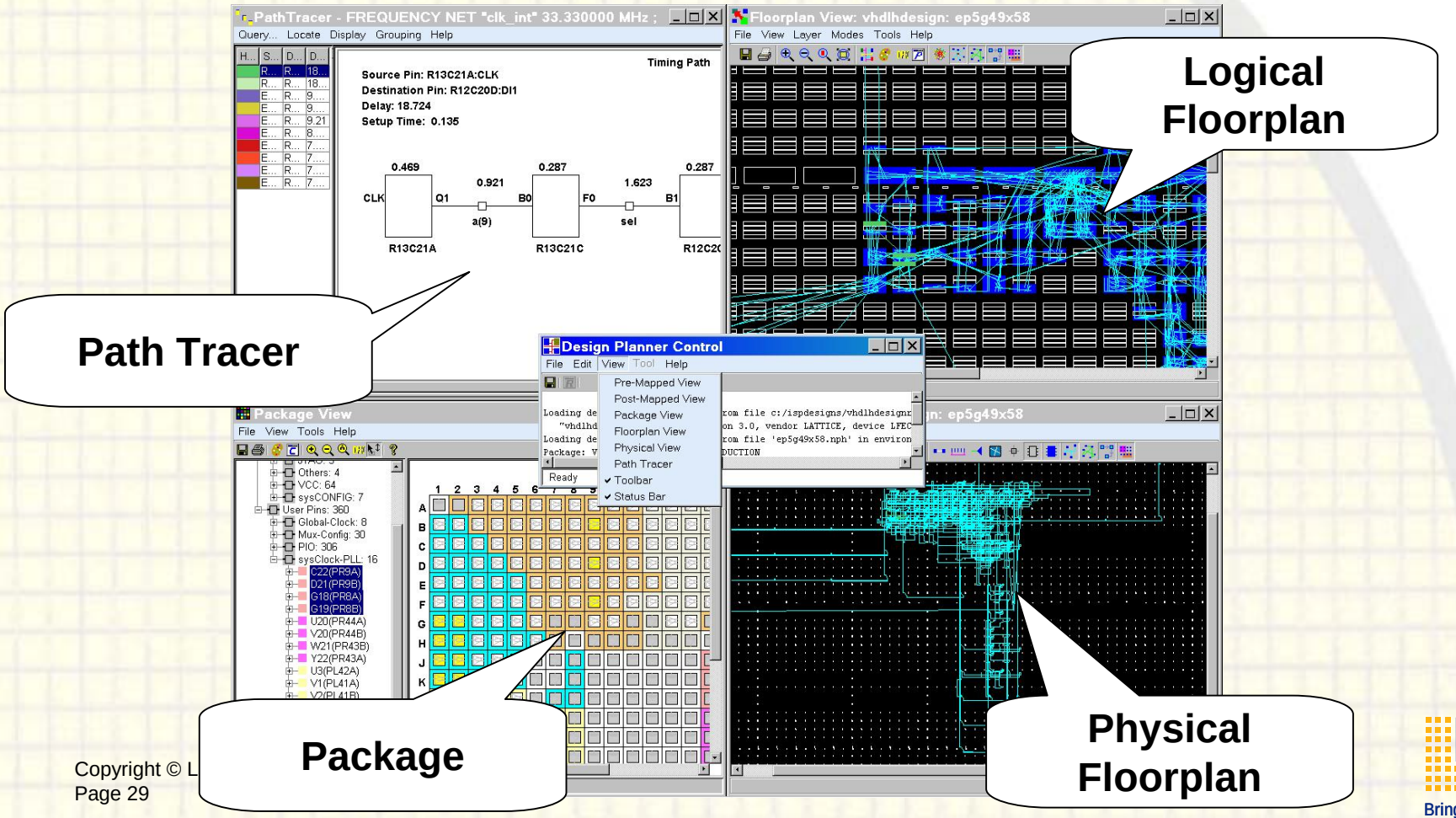
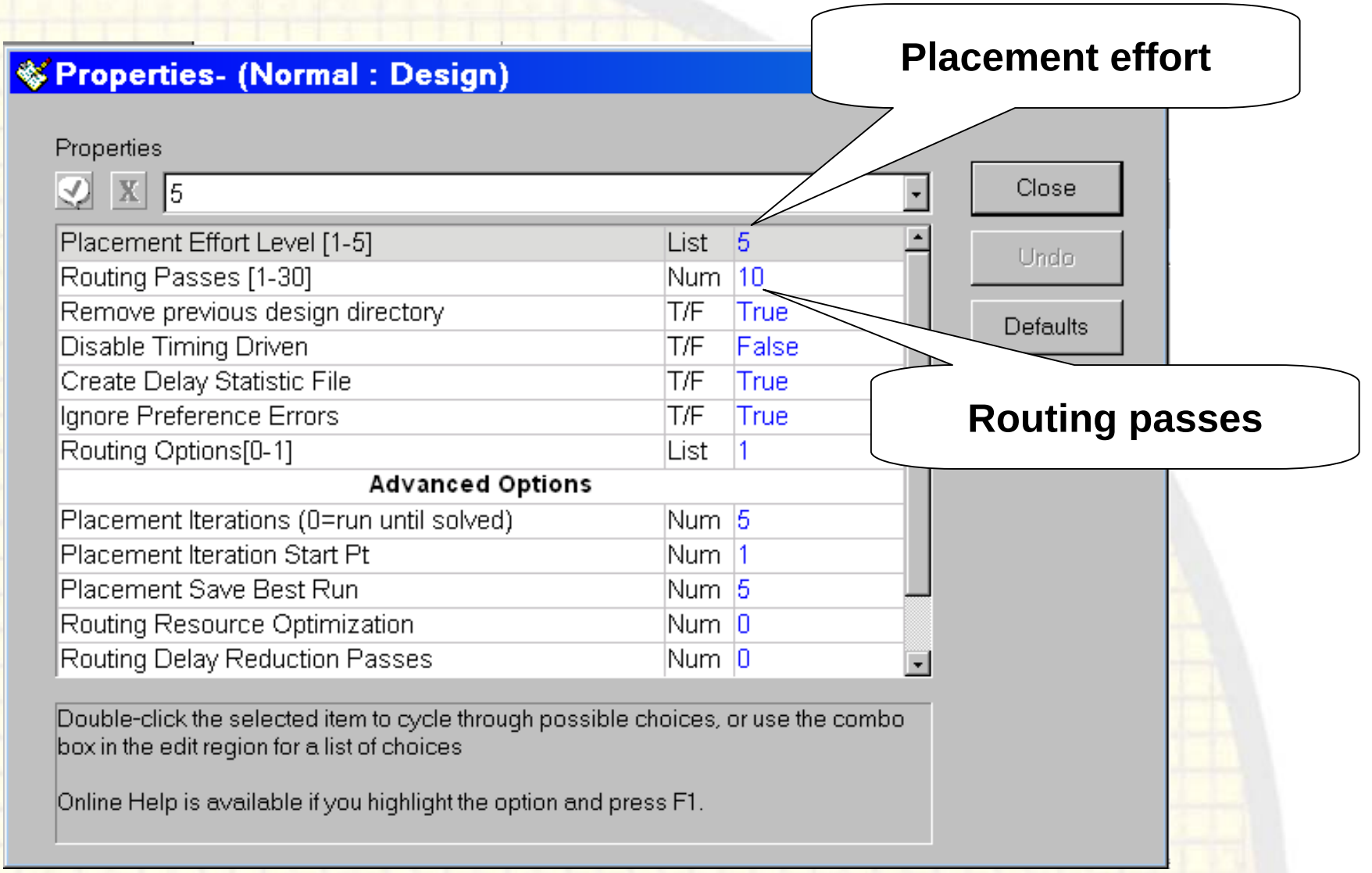
Design Planner: Floorplan & Package Views

- **Graphical Design Viewer and Editor**
  - **Used for Timing, Location, and Buffer Constraints**
  - **Used for pin assignment, grouping signals, placement, critical path analysis, routing analysis, … more**
  - **Useful in performance optimization and timing closure**

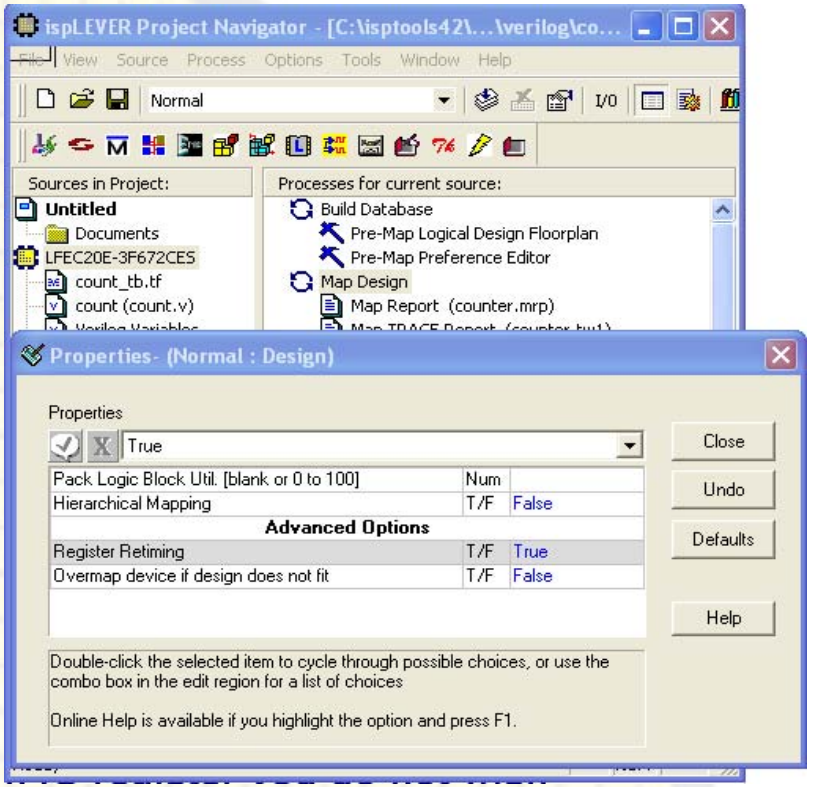


Place & Route Setup



Register Retiming

- **Balances Combinational Logic Across Register-Pairs**
  - **Maximizes f_{MAX} according to the constraints: t_{SU}, t_{CO} or f_{MAX} in preference file (.prf).**
- **Typically Improves f_{MAX} by 5-10%**
- **Controllable Option for Users**
- **"NOMERGE" Attribute in Verilog/VHDL**
  - **Added to each IO register where retiming is not desired**



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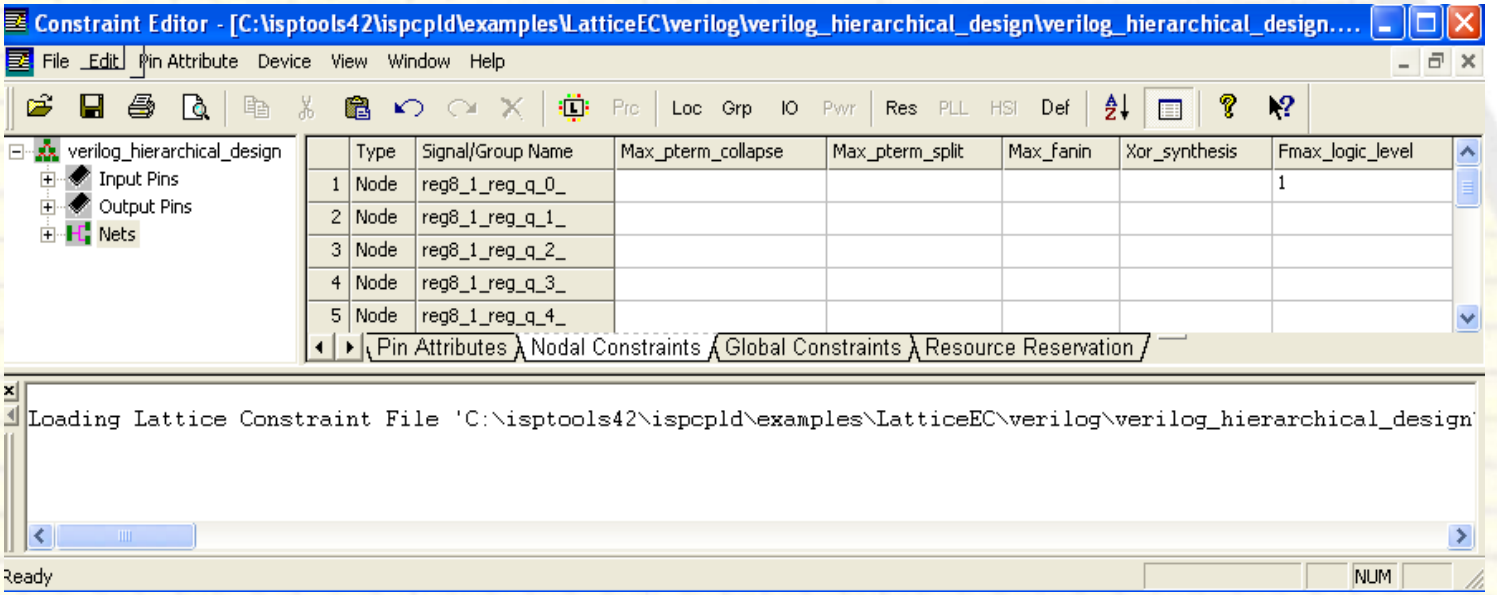
Nodal Control for CPLD

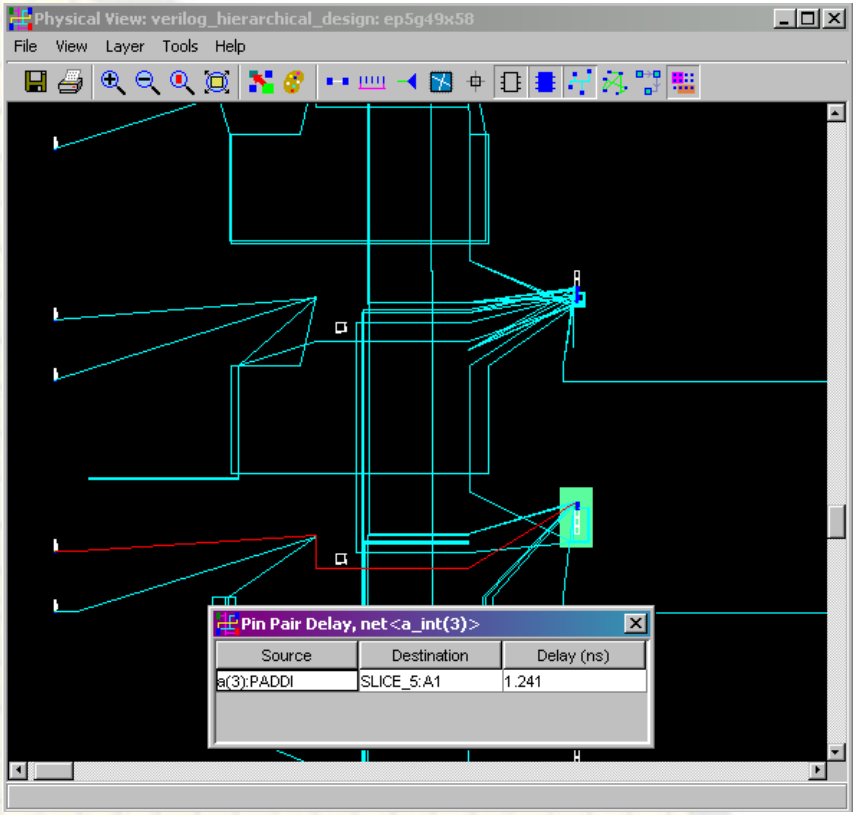
- **Constraints Added to Critical Nodes to Increase f_{MAX}**
  - **Decreases Levels of Logic → Improves Fmax**
  - **Limits PTERM usage**
  - **Limits Fanin**
  - **Takes advantage of XOR function**



EPIC – Device Editor

Tools for Device and Board Level Design Analysis

- Make Changes to NCD
- Place and route critical components before PAR
- Place and route critical signals after PAR
- Manually complete unrouted signals
- Perform Physical DRC
- Examine TRACE results
- Route buried signals to unused pins



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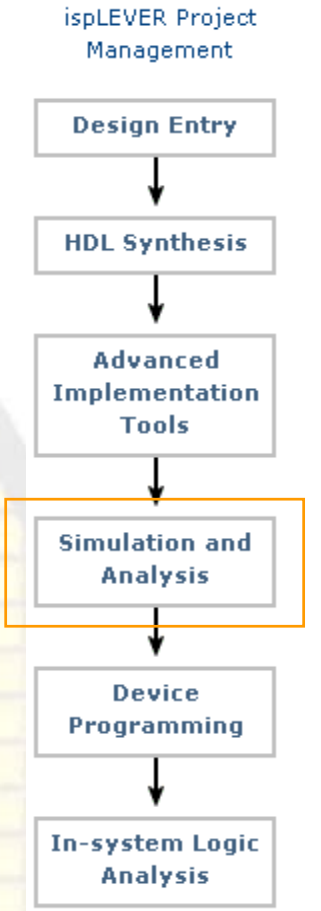
Simulation and Analysis

- **ModelSim for Lattice**
  - VHDL/Verilog/SystemVerilog language simulation
  - Tight script-based integration
  - Pre-compiled Lattice device library resources
  - Mentor Graphics Questa support available now
- **TRACE**
  - Timing Report and Circuit Evaluator
  - Constraints-driven Static Timing Analysis (STA)
  - Supports multi-cycle relationships and timing exceptions
- **Performance Analyst**
  - Easy to use tabular view for static timing analysis
- **Power Calculator**
  - Estimate AC and DC power consumption
  - Simulation data (VCD) import
  - Configure power supply requirements



Verify Function, Timing, and Power!

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ispLEVER Design Flow – Verification

Tools for Device and Board Level Design Analysis

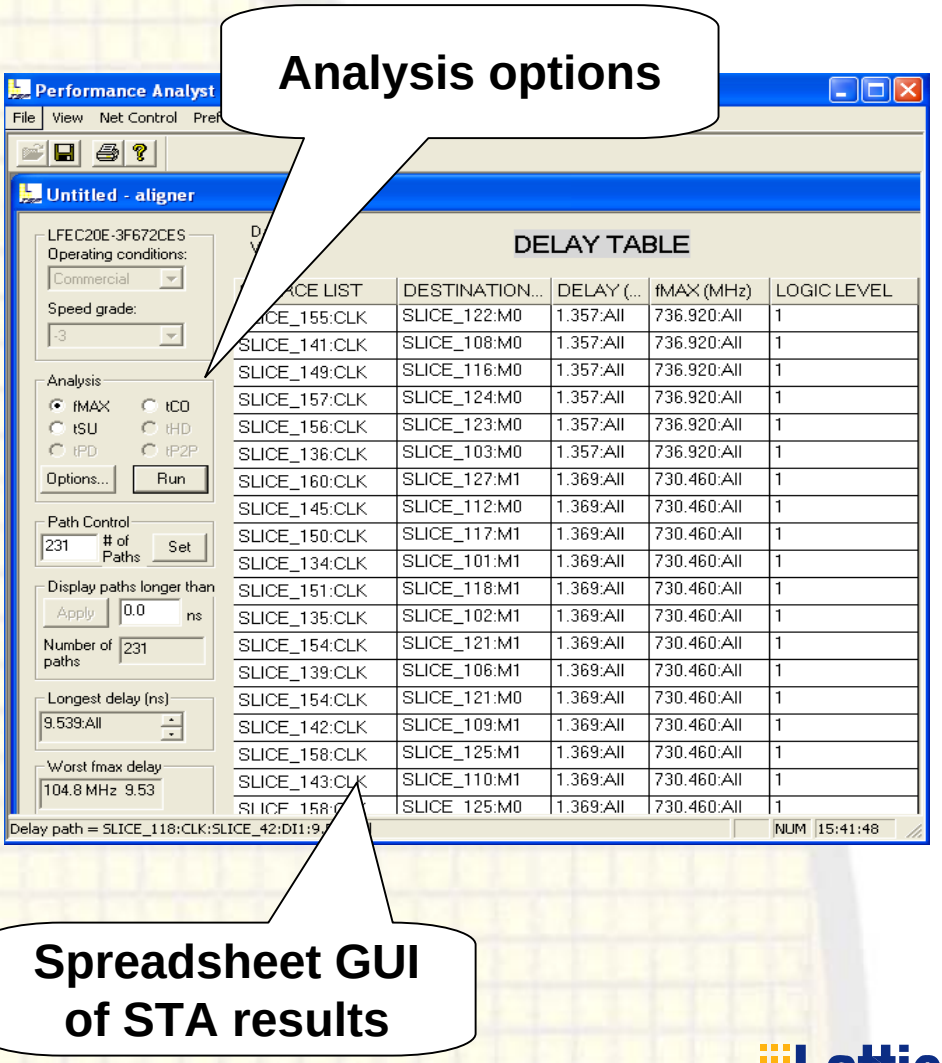
- **Static Timing Analysis (STA)**
  - Preference-driven STA
  - fMAX, tCO, tH
  - Multi-cycle
  - Timing exceptions
- **Timing Simulation**
  - Functional verification based on switching vectors to check for timing violations
- **Logic Analyzer**
  - Embedded logic analyzer with external probe points and triggers to capture internal (otherwise unobservable) signals
- **Power Estimation**
  - Accurately models device power consumption so that board power budgets may be checked
- **IBIS Modeling**
  - Signal integrity models to perform board level evaluation of noise and crosstalk generated on board level traces

TRACE Report – Static Timing Analysis

- TRACE = Timing Report and Circuit Evaluator
- Check Physical Design Delays
- Compares Against Timing Preferences
- Issues Timing Errors if Delays are Exceeded
- Used in Pre-Route and Post-Route Design Phases
- TRACE Timing Checkpoints May be Set
  - This is done in Project Navigator
  - Saves processing time by checking before long processing runs
- TRACE Report Provides:
  - Design statistics
  - Timing errors and warnings and their associated nets
  - Number of paths analyzed and percent coverage
  - Paths that cannot be analyzed

Performance Analyst – Static Timing Analyzer

- **Static Timing Analysis**
  - Looks at path delays without regard for signal switching
  - Facility for identifying critical paths
- **Search Facility**
  - Easily find specific signals
- **Filtering Features**
  - Unwanted nets, signals, etc., are <u>not</u> displayed
- **Supports All Devices**



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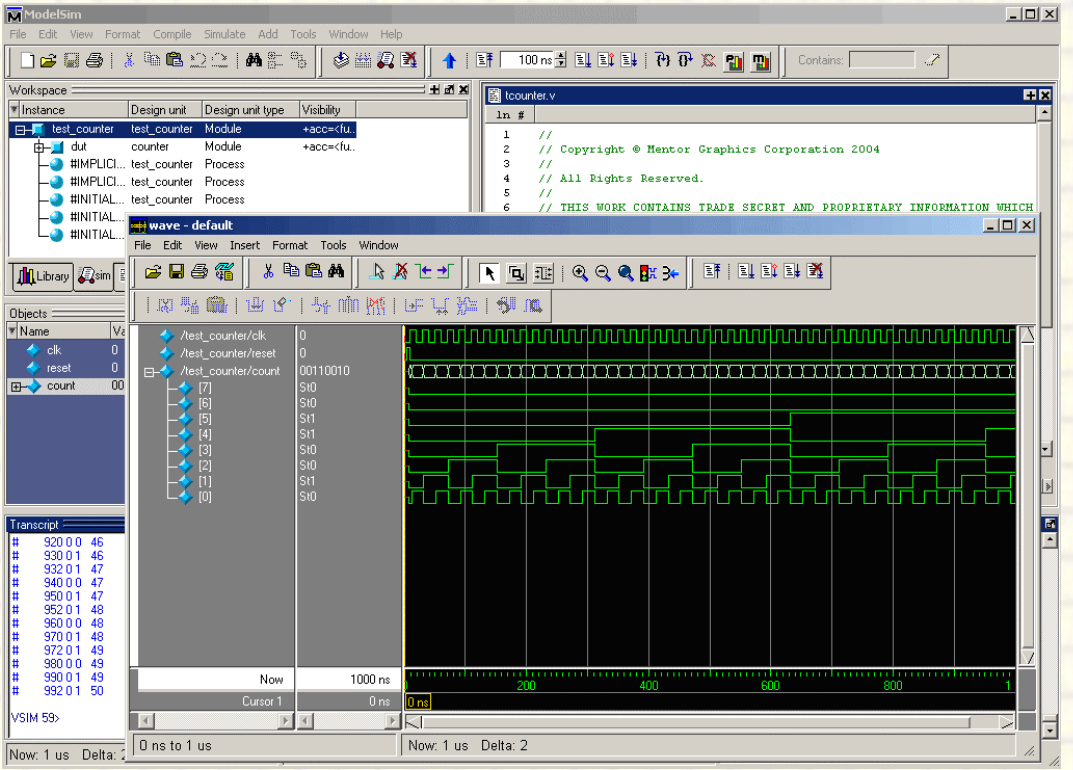
Mentor Graphics ModelSim – Timing Simulation

- **Critical for Checking Design Function as Signals Switch During Operation**
  - **Tests dynamic input vectors and validates against expected output**
  - **Critical for finding setup and hold time violations**
- **ModelSim is the De-facto Standard for FPGA Design**



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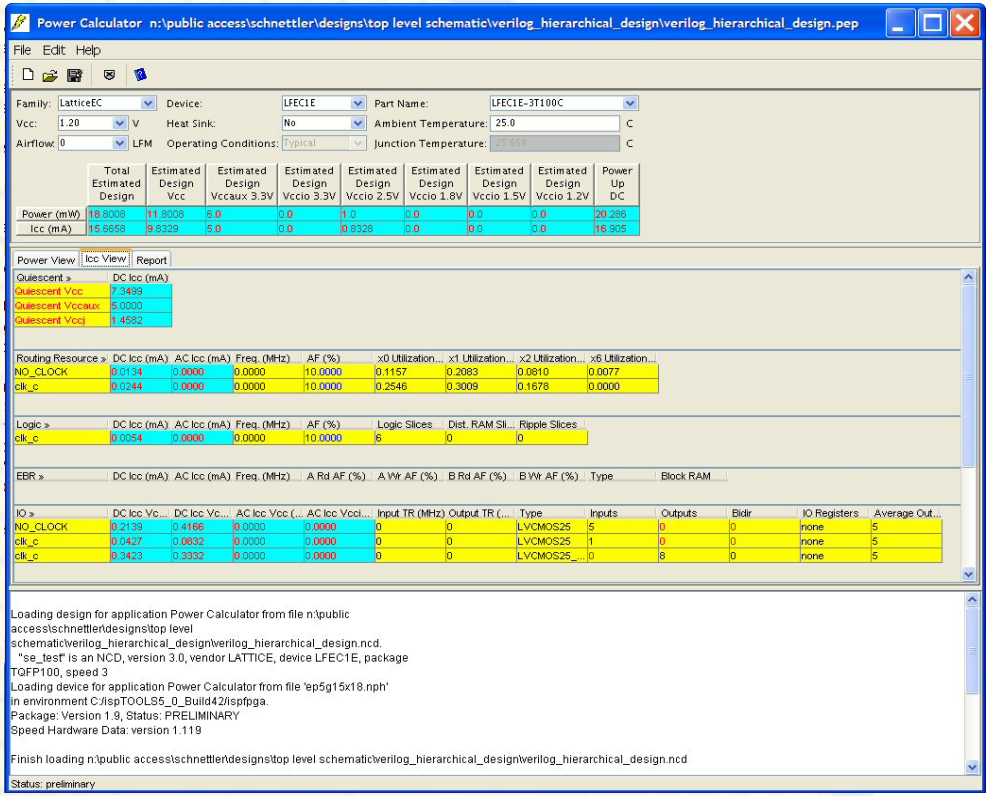
Power Calculator for FPGA

- Allows User to Determine Power Supply Requirements
- Toggle Rate Estimate Input
- VCD Import
- Total Power Summary Table
- Power and Icc Views
- XML Summary
- Parameters:
  - Airflow
  - Heatsink
  - Ambient temperature
  - Operating condition
  - Frequency



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ModelSim LATTICE

- **RTL and Gate-Level Simulation**
  - VHDL and Verilog Language Support
    - However, mixed languages NOT supported
    - Customer must buy mixed language support
- **De-facto Standard for FPGA Design**
- **NO RTL Line Limit in the Lattice OEM Version**
  - Very good performance
- **Included With ispLEVER (Windows) Package**
- **ispLEVER Automates "Do" File Creation**
  - Makes the simulation easier to set up and use

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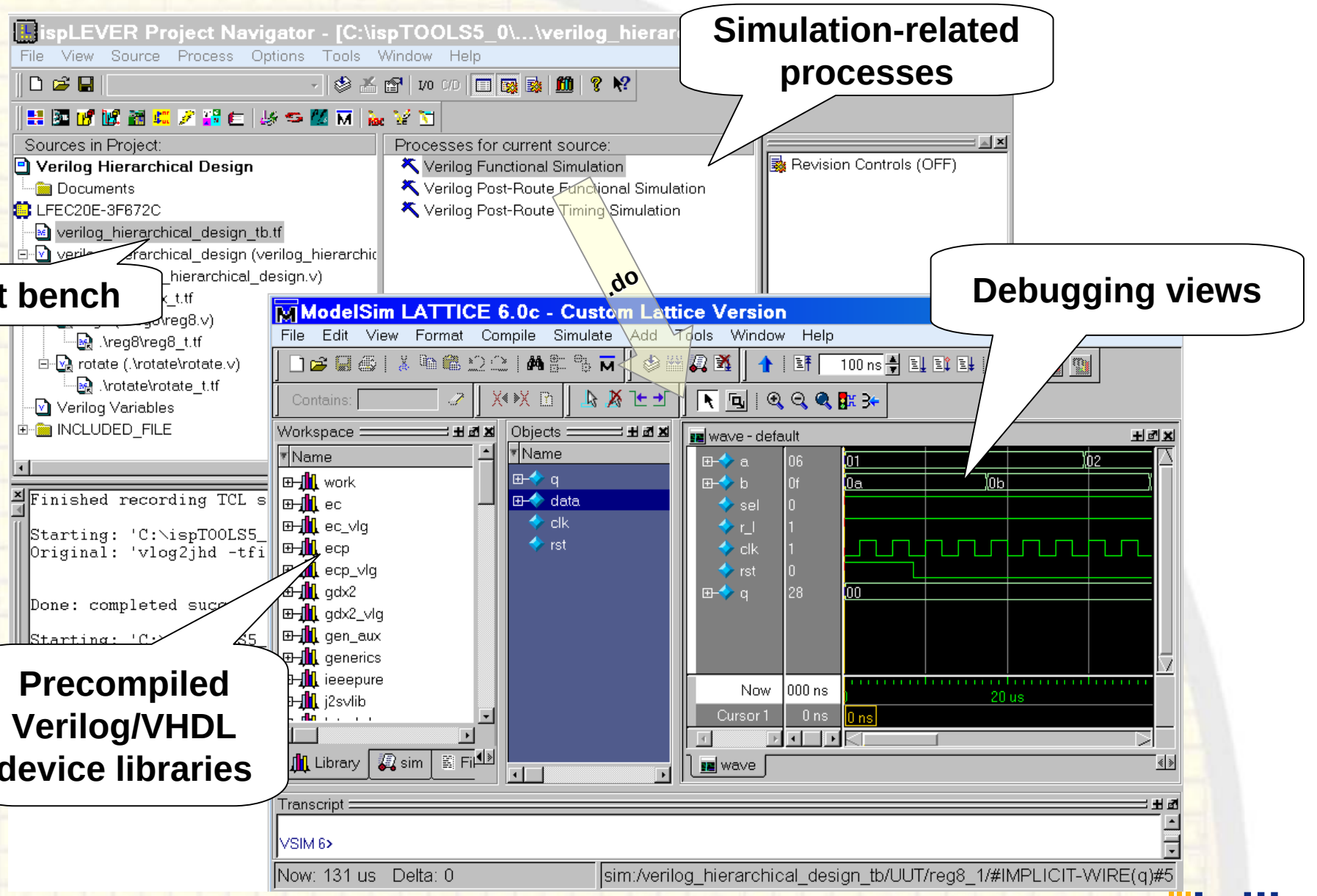
ModelSim Integration



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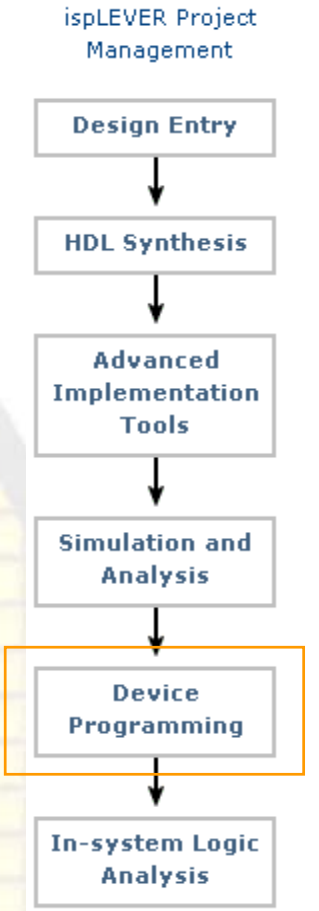
Device Programming

- **Supports All Lattice Devices**
  - IEEE 1149.1 in-system programming
  - SPI Flash programming support
  - TransFR support
  - Multiple programming format support
    - » ISC BSDL/Data, SVF, JEDEC, IEEE 1532, etc.
  - Format translation, Universal File Writer (UFW)
- **ispVM Embedded**
  - Device programming via embedded processors
  - VME source code provided
- **Serial Vector Format (SVF) Debugger**
- **ATE Programming Vector Generator**
- **USB Gang Programming (DLxConnect)**



Industry's Best Programming Solution!

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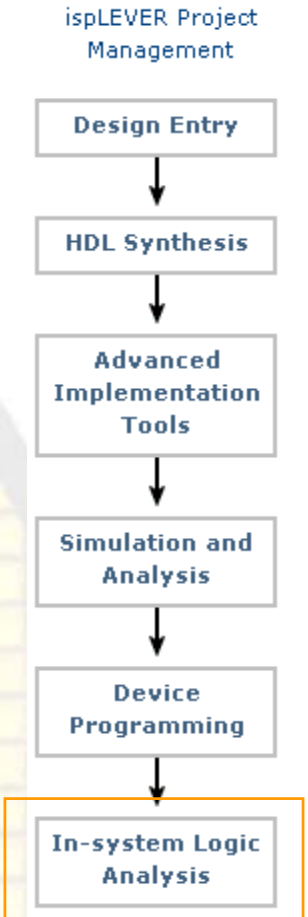
In-System Logic Analyzer

- **Embedded Logic Analyzer Core**
  - **Configure trigger logic and trace buffer via IPexpress**
  - **Easy LA-to-logic connection GUI**
  - **Non-invasive (HDL), post-synthesis core integration (EDIF)**
- **ispTRACY Logic Analyzer**
  - **User defined triggers and capture modes**
  - **List or wave format analyzer GUI**
  - **Integration with ispVM**



Real-Time Logic Analysis!

ROADMAP ITEM

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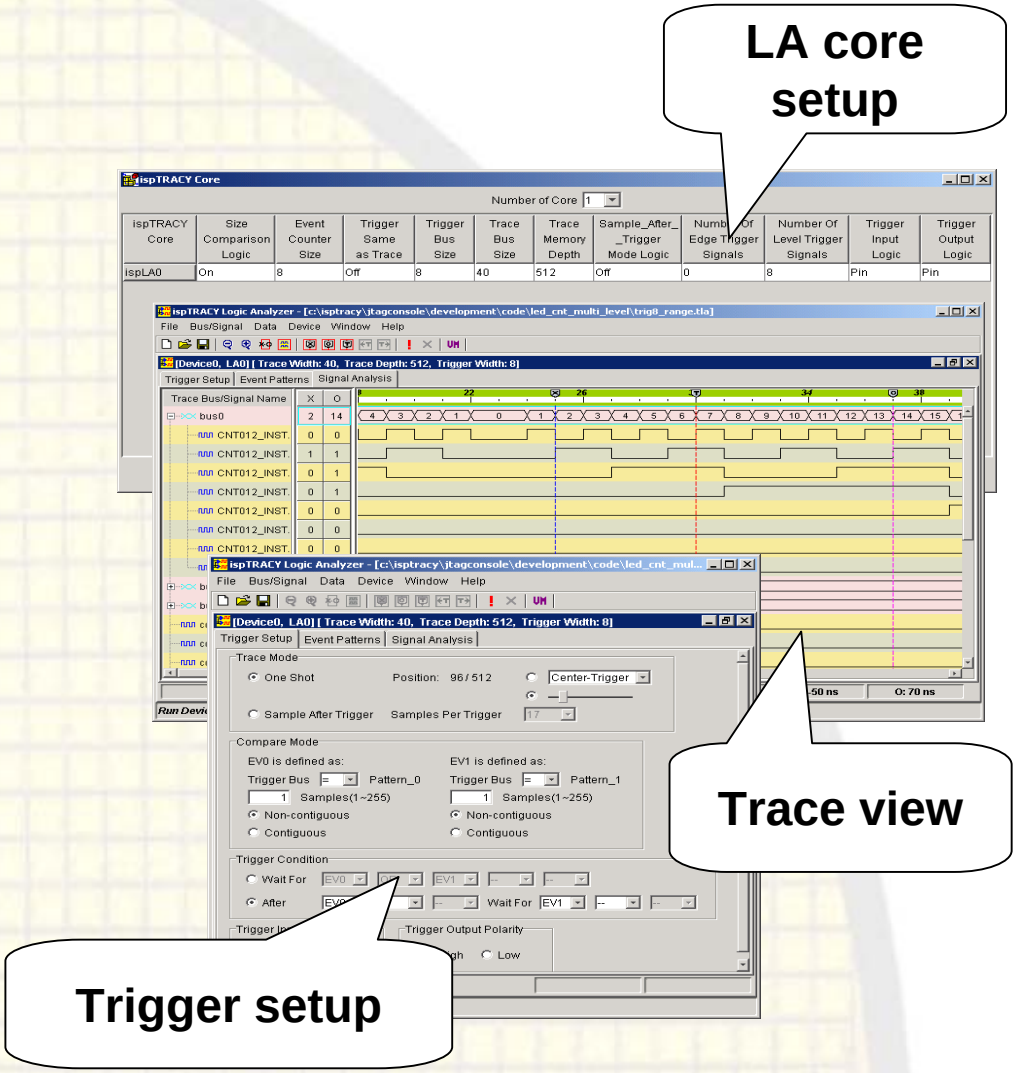
ispTRACY – Logic Analyzer

- Embedded Logic Analyzer IP core
- Logic Analyzer UI
- Set triggers
- Select capture modes
- Enable external trigger input and output
- Run or stop the triggers
- Waveform and List Display
- Post Synthesis (EDIF) integration of IP cores
- Multiple device analysis
- Improved signal markers
- New TRST settings



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CAE Tool Support

- **OEM Tools**
  - ModelSim for Lattice
  - Synplify for Lattice
  - Precision RTL Synthesis for Lattice

- **Key 3rd Party Interface Options**
  - MathWorks MATLAB/Simulink
  - Mentor Graphics Questa (Sim)
  - Cadence NC-Verilog (Sim)
  - Synopsys VCS (Sim)

- **3rd Party Options**
  - Aldec Active-HDL (Capture and Sim)
  - Aldec Riviera (Sim)
  - Altium Nexar (Capture and Sim)

Outstanding 3rd Party Support!

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PCB/CAD Tool Support

- **Lattice Model Resources**
  - **IBIS (I/O Buffer Information Specification)**
    - » **EDA tools: Mentor Graphics HyperLynx, Zuken CADSTAR, etc.**
    - » **Signal integrity (SI) simulation (<1GHz)**
  - **SPICE**
    - » **Signal integrity (SI) simulation (>1GHz)**
    - » **Requires factory NDA and Synposys HSPICE**
  - **BSDL (Boundary Scan Description Language)**
    - » **Boundary scan chain models describe devices in a JTAG-compatible scan chain**
- **ispLEVER File Exports**
  - **Comma Separated Value (CSV) pin reports**
    - » **EDA tools: OrCAD, Protel, etc.**
  - **Design-specific IBIS export**
  - **OrCAD Capture CPLD pin reports**

Outstanding 3rd Party Support!

IBIS Model Generation

- **Design Specific Signal Integrity Model**
  - **Uses a base "template" IBIS model for each family**
  - **Generates specific model of user's design based on resources used**
- **Useful For Board Level Signal Integrity Verification**
  - **Crosstalk**
  - **Noise**
  - **Signal loss over long traces**

ispLEVER 6.0 (Plus SP1) - What's New?

- LatticeECP2-50
  + ECP2-12 in SP1
  (Preliminary Timing)
- LatticeSC15, 25, and 80
  (Contact Lattice)
- IPexpress Web Interface
- Design Planner
  - Easier and faster I/O planning
  - Advanced floorplanning and preference editing
- Schematic Library For FPGA
- DSP Design Enhancements
  - Device support for: ECP2, SC/SCM, EC, XP, and XO
  - MATLAB/Simulink reference designs
  - Floating to Fixed point conversion tutorial
- Aldec, Cadence, and Synopsys simulators qualified
- Expanded Precision RTL and Synplify Controls
  - TCL Format project files
  - Easier report access
  - Expanded tool controls
- CPLD Pin Export for OrCAD Capture
- Project Navigator: Top-Level HDL/Schematic Module Selector
- Text Editor: HDL Template Preview
- Power Calculator: Command line interface
  - Updated in SP1 to improve accuracy
- Precision RTL Synthesis 2005C Update 2
- ModelSim LATTICE 6.1D
- Synplify for Lattice 8.6A

Agenda

- ispLEVER Software Feature Overview
- ispLEVER Versus the Competition
- ispLeverCORE Overview
- PAC-Designer Software Feature Overview
- Development Hardware
- How to Learn More

Software Orientation

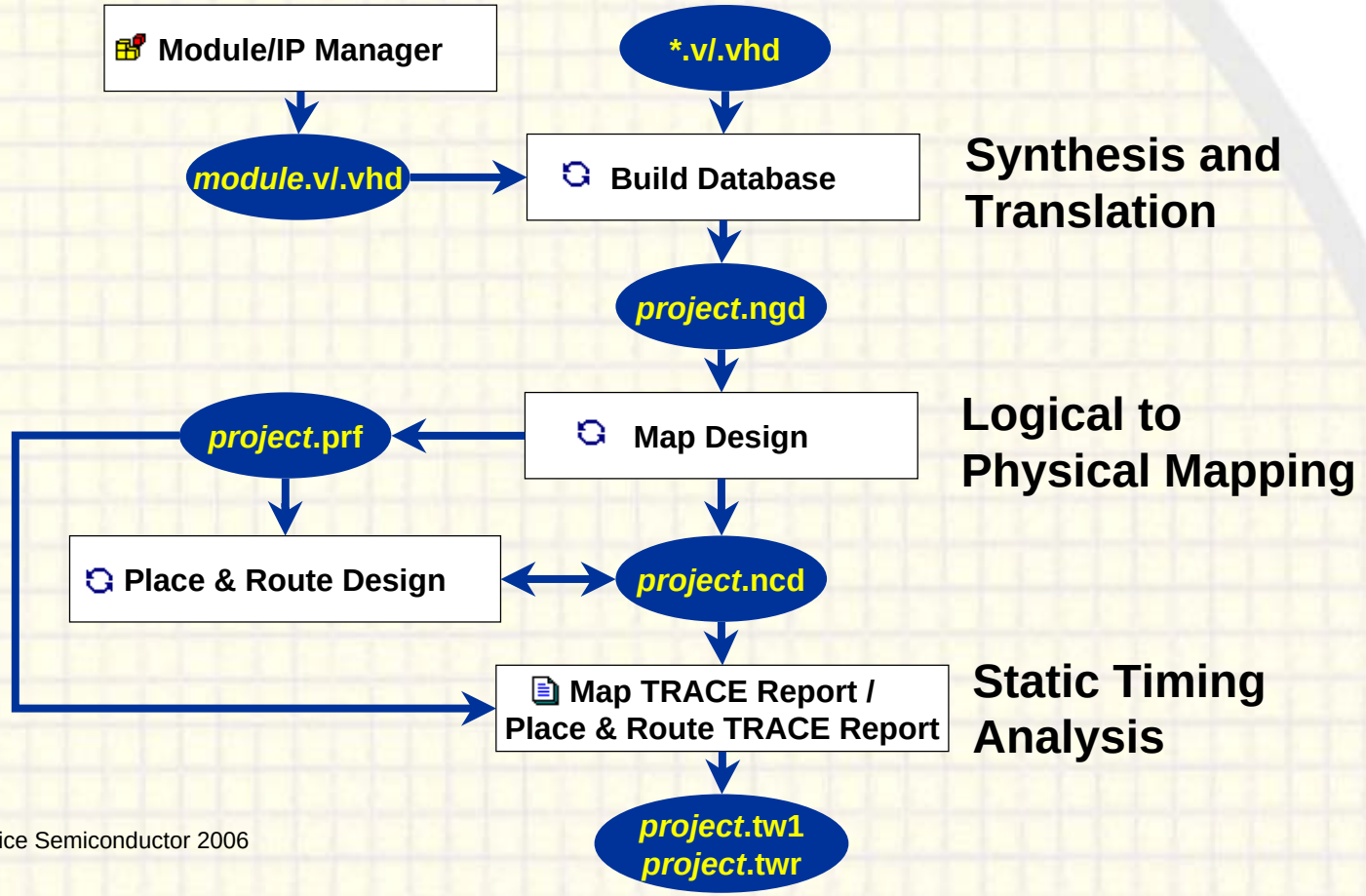
	ispLEVER	ISE	Quartus II
Design Entry	Project Navigator Block Modular Design Text Editor Schematic Editor IPexpress Design Planner Design Planner	Project Navigator Modular Design HDL Editor ECS CORE Generator Constraints Editor Floorplanner	Project Navigator LogicLock Text Editor Block Editor MegaWizard Plug-In Mgr Assignment Editor Floorplan Editor
Functional Simulation	ModelSim or 3RD party simulation tools Waveform Editor	ModelSim or 3RD party simulation tools	Simulator or 3RD party simulation tools Waveform Editor
Power Estimation	Power Calculator	XPower	PowerPlay

Software Orientation

	ispLEVER	ISE	Quartus II
Design Implementation	Precision RTL or Synplify NGDBUILD MAP PAR	XST or 3rd party NGDBUILD MAP PAR	QII Integrated Synthesis or 3rd party Fitter
Timing Analysis	TRACE and Performance Analyst	TRACE and Timing Improve. Wiz.	Timing Analyzer
Programming Configuration	BITGEN ispVM	BITGEN iMPACT	Assembler Programmer
On-Chip Debugging	ispTRACY	ChipScope	SignalTap II

Migrating a Xilinx ISE User to ispLEVER

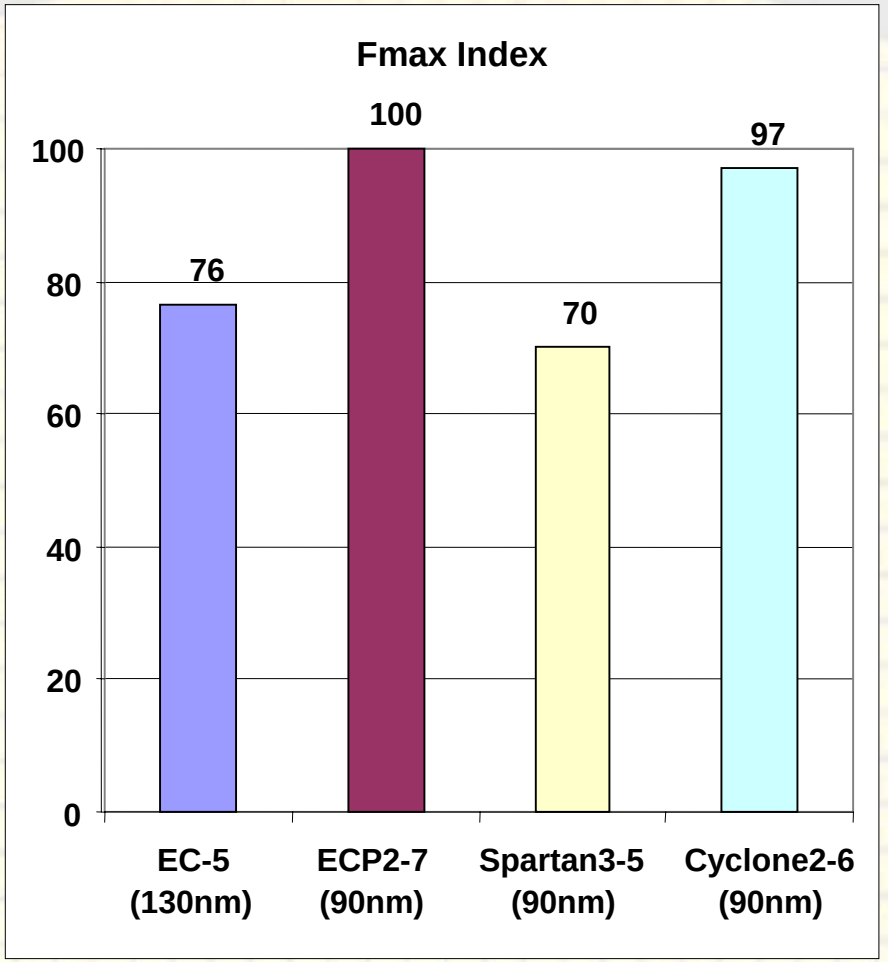
- Includes industry standard synthesis tools
- Includes ModelSim
- Many similarities: MAP, PAR, TRACE, and EPIC

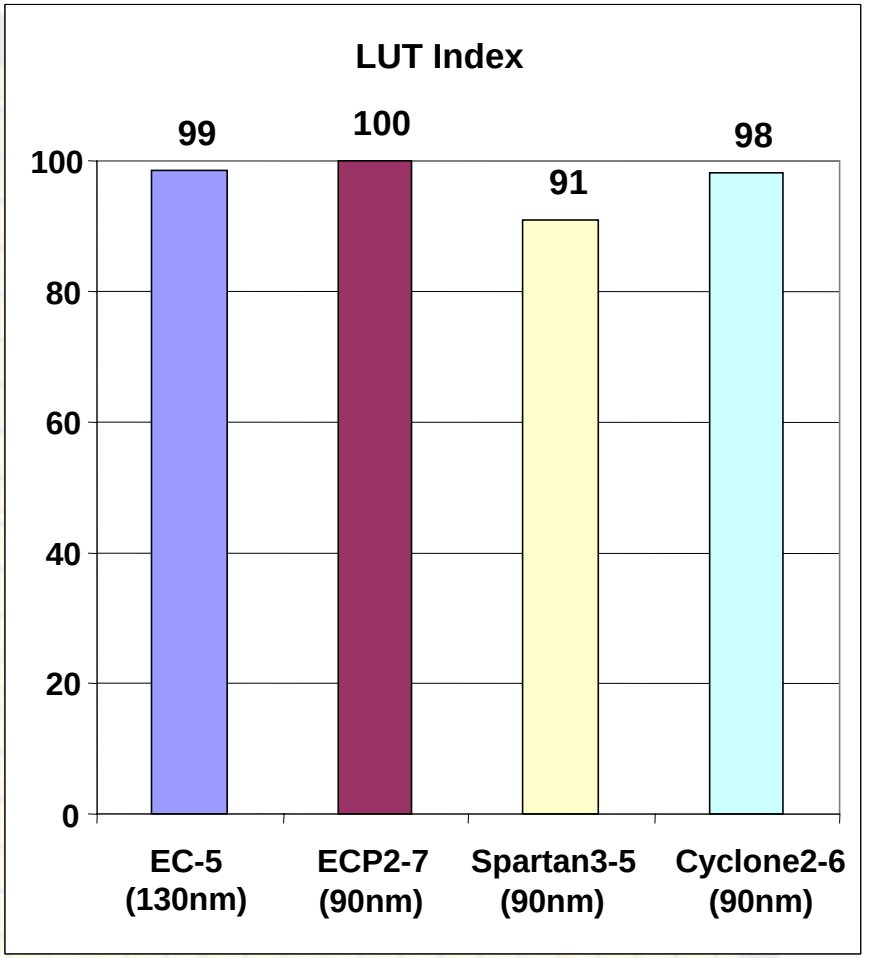


Migrating FPGA Designs

- FPGA Design Guide
  - Chapter 2: FPGA Design for Altera Users
  - Chapter 3: FPGA Design for Xilinx Users
- Replace Library
- Replace Specific Primitives in Source with Equivalent Primitives
- Replace Modules
- Replace Constraints with Preferences
- Optimize HDL-Inferred Modules

LatticeECP/2 – Performance Advantage!





- Average of benchmark designs using high effort
- Tools used: ispLEVER 6.0.00.24, Synplify 8.5d(OEM); Xilinx ISE 8.1SP1, SynplifyPro 8.2; Altera Quartus 5.0SP1, SynplifyPro 8.2
- Command line: Map, Place, Route, and Timing Report
- Machine used: Pentium4 2.8 GHz, 2 GB, Windows 2000
- ECP2–7; EC-5; Spartan3-5; Cyclone2–6

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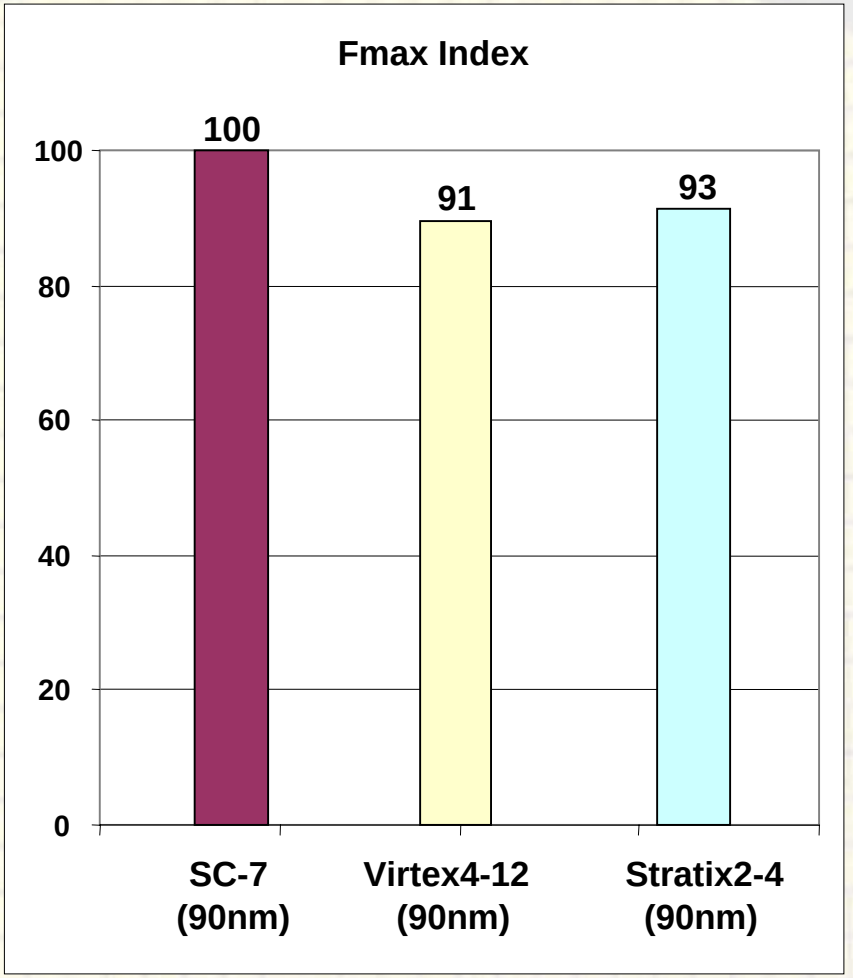
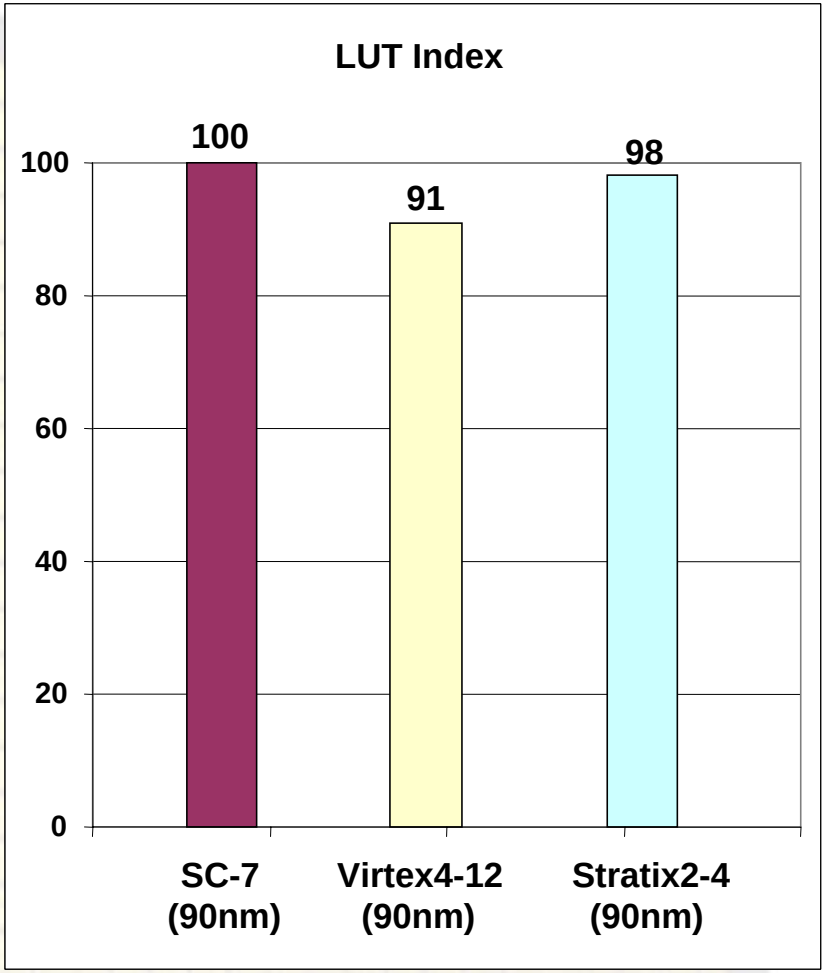
LatticeSC Family – Performance Advantage!





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- ECP2–7; EC-5; Spartan3-5; Cyclone2–6

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Conclusion

- Complete Solutions for All Your Needs
- Industry Leading Synthesis and Simulation Tools
  - From Mentor Graphics and Synplify
- Easy to Use and Easy to Learn
- Familiar Flow and File Extensions
- Unsurpassed Performance and Productivity
- Industry's Best Value

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Agenda

- ispLEVER Software Feature Overview
- ispLEVER Versus the Competition
- ispLeverCORE Overview
- PAC-Designer Software Feature Overview
- Development Hardware
- How to Learn More

IP Core Portfolio

- **Downloadable Reference Designs**
  - **www.latticesemi.com**

- **ispLeverCORE IP**
  - **Lattice Semiconductor Corp**

- **ispLeverCORE Connection Partners**
  - **CAST**
  - **Digital Core Design (DCD)**
  - **Elliptic**
  - **Eureka Technologies**
  - **Northwest Logic**

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ispLeverCORE IP

- **Available for Purchase from Lattice**
  - Evaluation version available for download from the Lattice website
  - Netlist or Source available
  - Board or Site licenses
- **Includes:**
  - Description
  - Features summary
  - Configurations available
  - User's Guide
  - Evaluation capability
  - Tech Note / Brochure (selected functions)
- **Where to Find the List of IP Available**
  - Search screen:

    http://www.latticesemi.com/products/intellectualproperty/

43 Unique Functions

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Reference Designs

- **Available for Download from Lattice Website**
  - Free of charge
- **Includes:**
  - Description
  - Features summary
  - Configurations Available
  - User's Guide
  - Source Code
  - Tech Note / Brochure (selected functions)
  - Demonstration design (selected functions)
- **Where to Find the List of Reference Designs**
  - Search screen:

    http://www.latticesemi.com/products/intellectualproperty/

28 Unique Functions

ispLeverCORE Connections Partners

- 3rd Party Developed, Sold, and Supported
- Augments The Lattice Portfolio
  - Adds functions for applications for which we have little experience or expertise
- Leverage 3rd Party Expertise
  - Experts create and support complex functions
- Faster Time to Market
  - 3rd Parties act as resources to port and support

CAST

DIGITAL CORE DESIGN

Eureka Technology

NORTHWEST LOGIC

Elliptic Semiconductor

art of silicon

Look for this Approved logo on all ispLeverCORE Connection IP Products.

ispLeverCORE Approved

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LatticeMico8 – 8-Bit Microcontroller

- **Optimized For Lattice Leading-Edge Families**
  - LatticeECP/EC, LatticeXP, and MachXO
- **Targeted Towards Wide Variety Of Applications**
  - Consumer, Computation, Communications, Medical, Industrial, Auto
- **Innovative Open IP Core License**
- **Key Architectural Features**
  - 8-Bit Data Path
  - 18-Bit Wide Instructions
  - Two Cycles Per Instruction
  - 32 General Purpose Registers
  - 32 Bytes Of Internal Scratch Pad Memory
  - Input/Output Is Performed Using Ports (Up To 256 Port Numbers)
  - Optional 256 Bytes Of External Scratch Pad RAM
  - Lattice UART Reference Design Peripheral
- **Source, Documentation, Everything Needed for Design**

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Agenda

- ispLEVER Software Feature Overview
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- PAC-Designer Software Feature Overview
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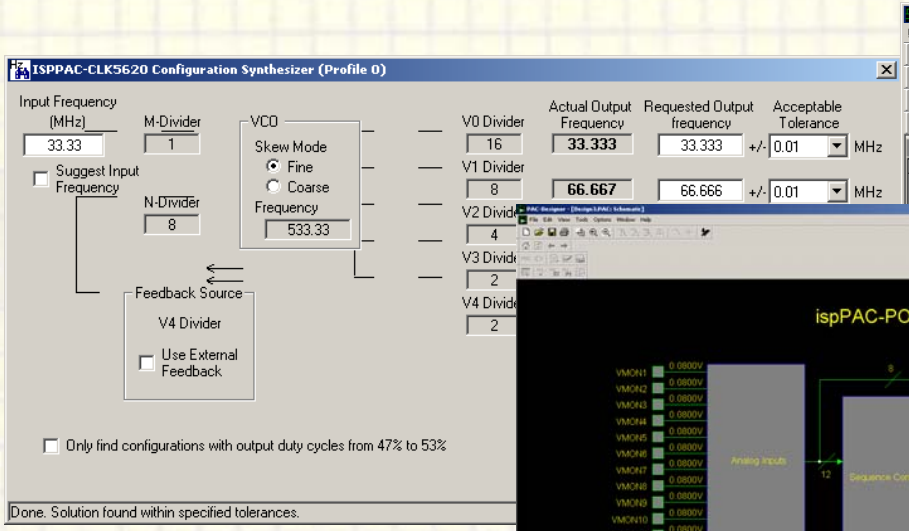
- How to Learn More

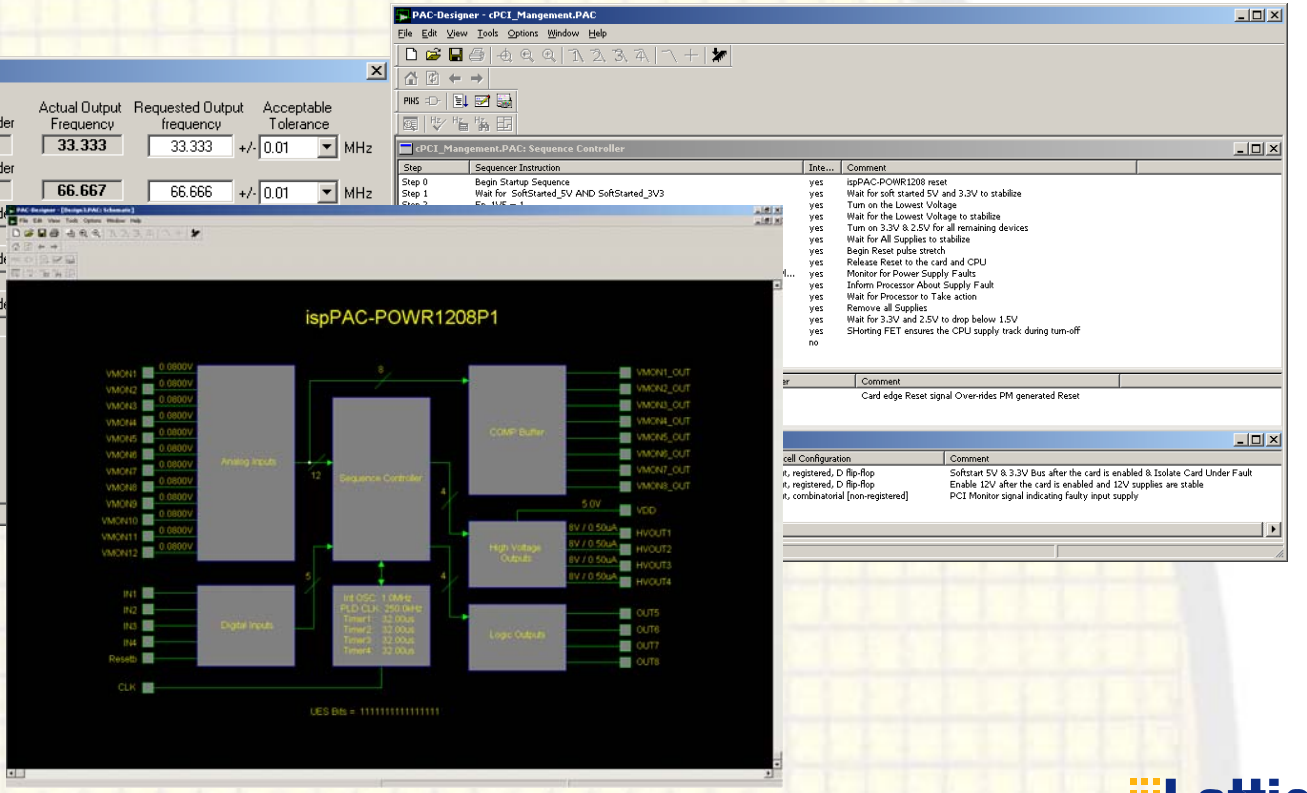
PAC-Designer – Mixed Signal Design Tool

- Complete Mixed Signal Design Tool
- Self Contained Support for All ispPAC Devices:
- Fully Integrated Design and Simulation Environment
- High Level Logic Design Mechanism

LogiBuilder for CompactPCI



Frequency Synthesizer



PAC-Designer GUI for ispPAC Power Manager

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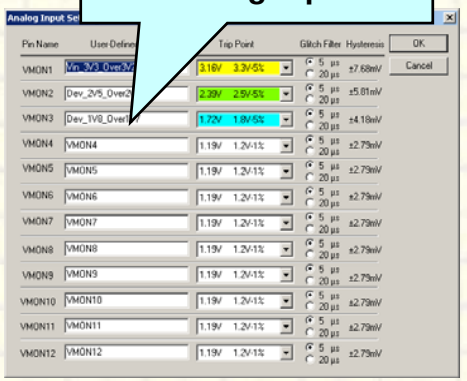
PAC-Designer – Design Tool Features

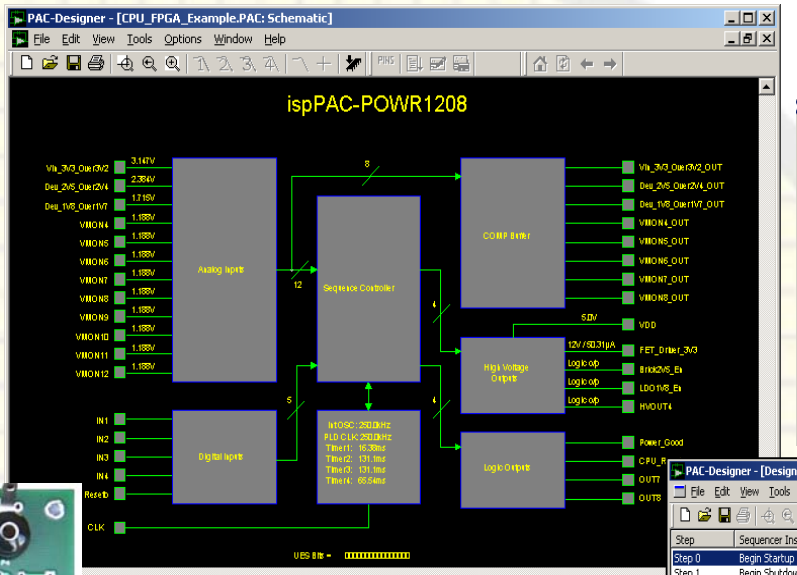
- Easy-to-use GUI
- SPICE model export
- Design Entry
  - LogiBuilder, Hierarchical design entry, High level design entry power management, Standard circuit generation library
- Design Utilities
  - Clock frequency synthesis, Graphical skew editing, Frequency calculators
- Simulation
  - Create stimulus graphically, Digital Waveform simulation, View both gain and phase plots graphically, Simultaneously view inputs and outputs, Cross-hair cursors to directly read any gain or phase magnitude
- Facilitates Manufacturing Automation
  - Library of automation functions, Circuit board for different, Example program and documentation

Complete Power Management Design in 5 Steps

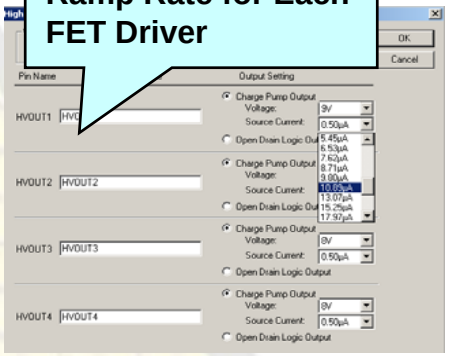
Lattice PAC-Designer Software

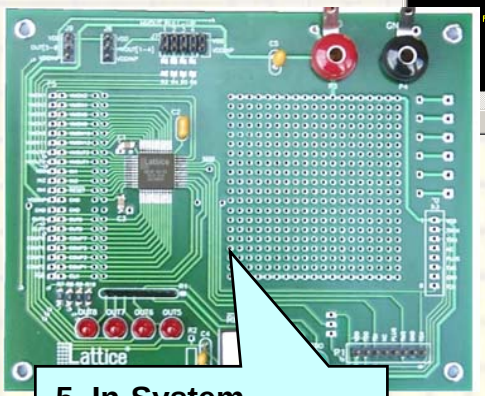
1. Set Power Supply Threshold For Each Analog Input



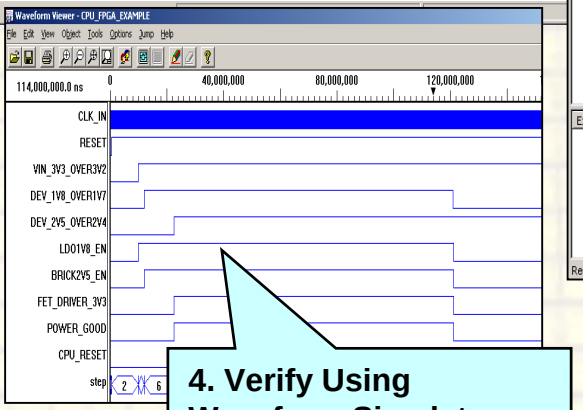


2. Set Power Supply Ramp Rate for Each FET Driver

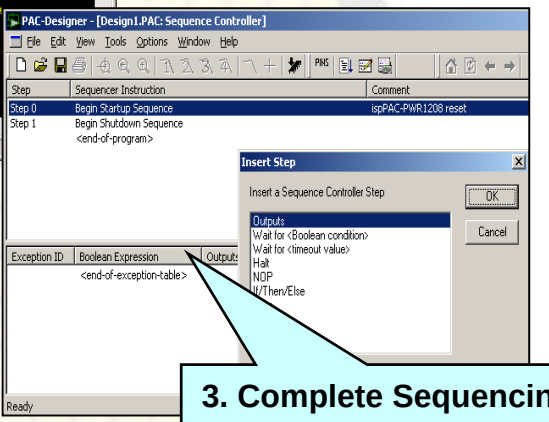




5. In-System Program the Design Through JTAG



4. Verify Using Waveform Simulator



3. Complete Sequencing and Monitoring Design Using LogiBuilder

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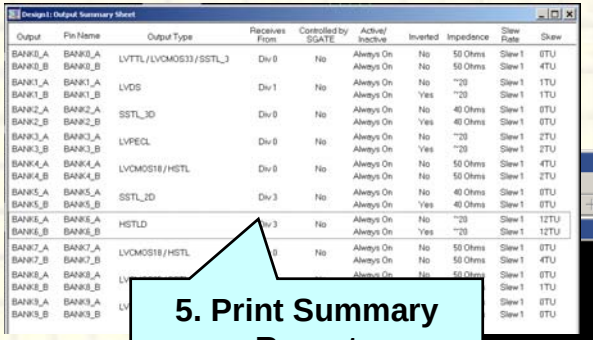
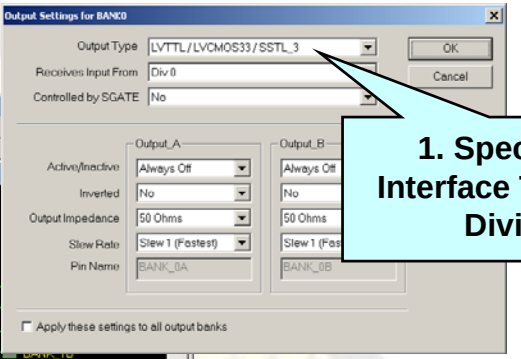
Complete Clock Net Design in 5 Steps

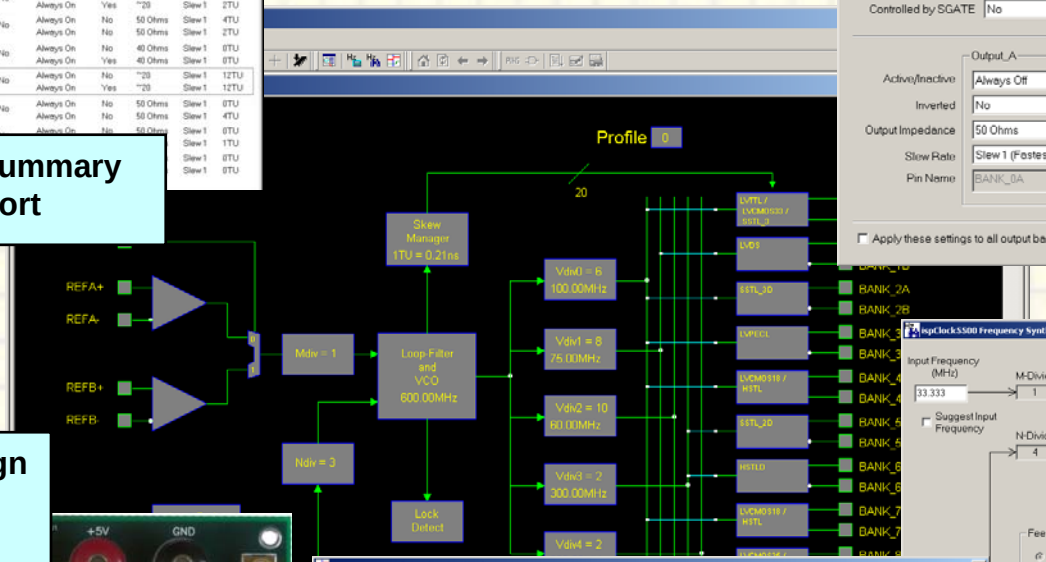


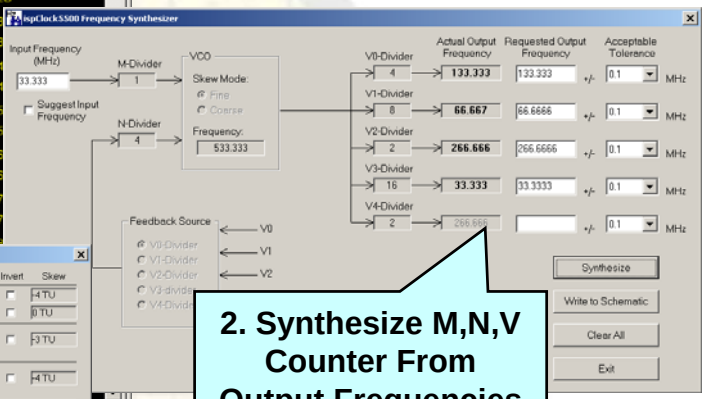
5. Print Summary Report

Lattice PAC-Designer Software



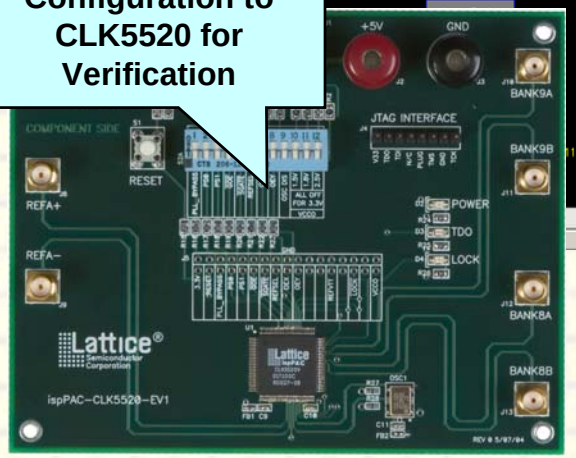
1. Specify I/O Interface Type and Divider

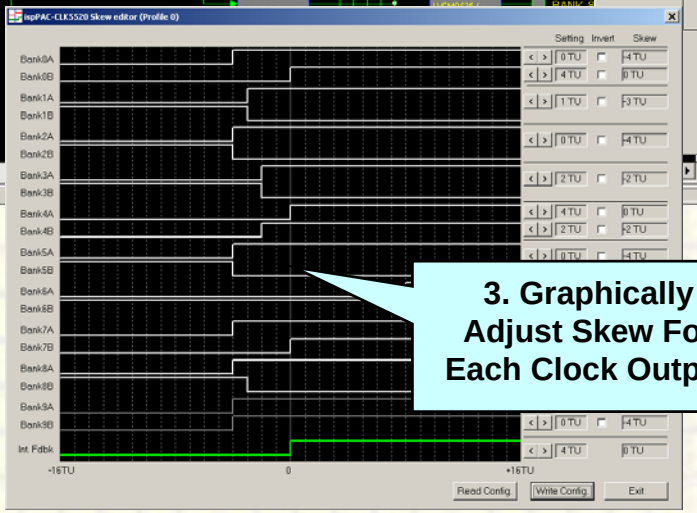




2. Synthesize M,N,V Counter From Output Frequencies

4. Download Design Configuration to CLK5520 for Verification





3. Graphically Adjust Skew For Each Clock Output

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Agenda

- ispLEVER Software Feature Overview
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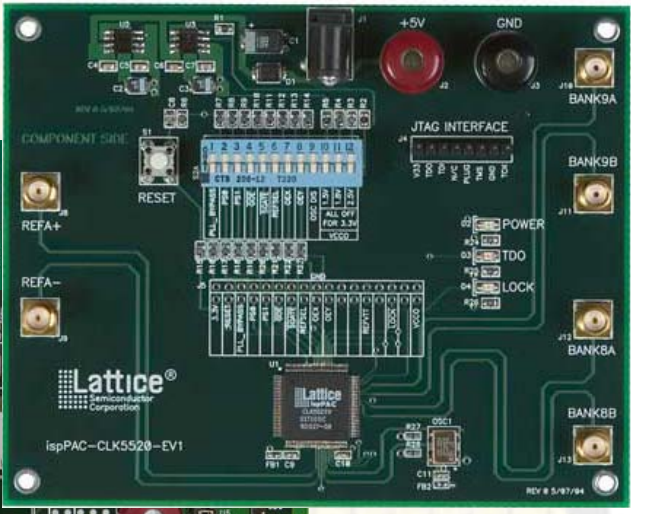
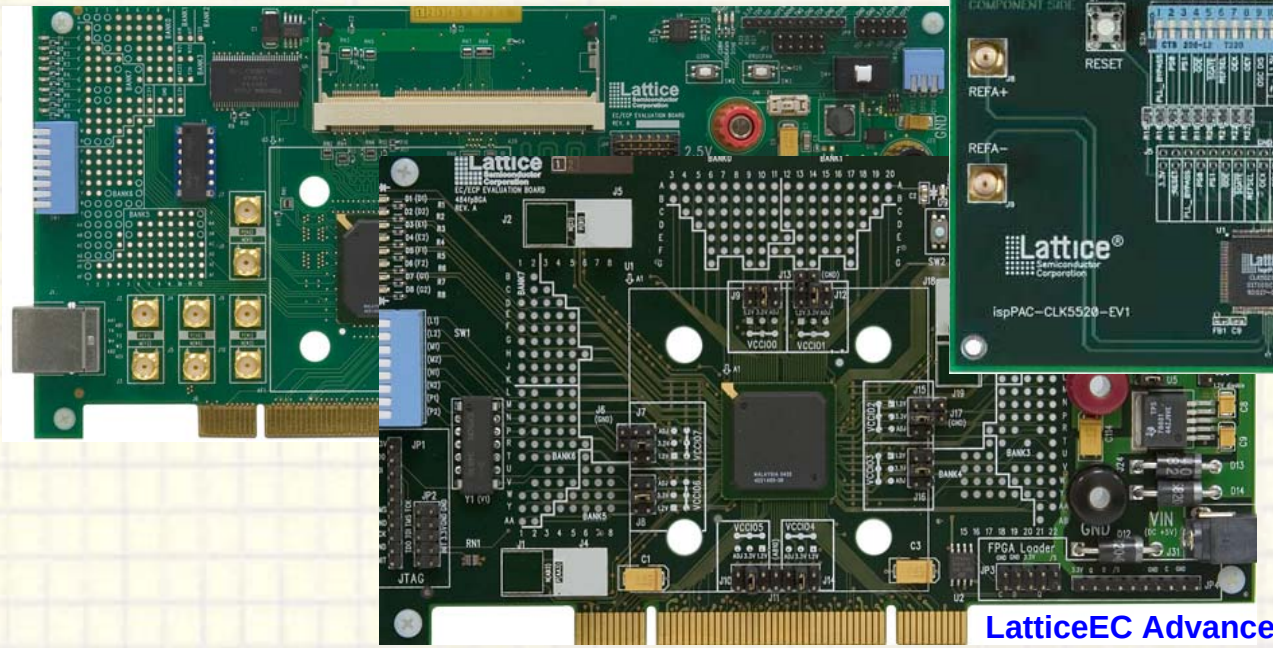
Evaluation Boards

- **Wide Range of Evaluation Boards**
  - **LatticeSC / ECP2 / ECP-DSP / EC / XP / XPGA FPGAs**
  - **Lattice MachXO Crossover PLD**
  - **Lattice ORCA FPSCs**
  - **ispMACH 4000 / ispXPLD CPLDs**
  - **ispPAC / ispCLOCK**

ispCLOCK Evaluation Board



LatticeEC Standard Evaluation Board



LatticeEC Advanced Evaluation Board

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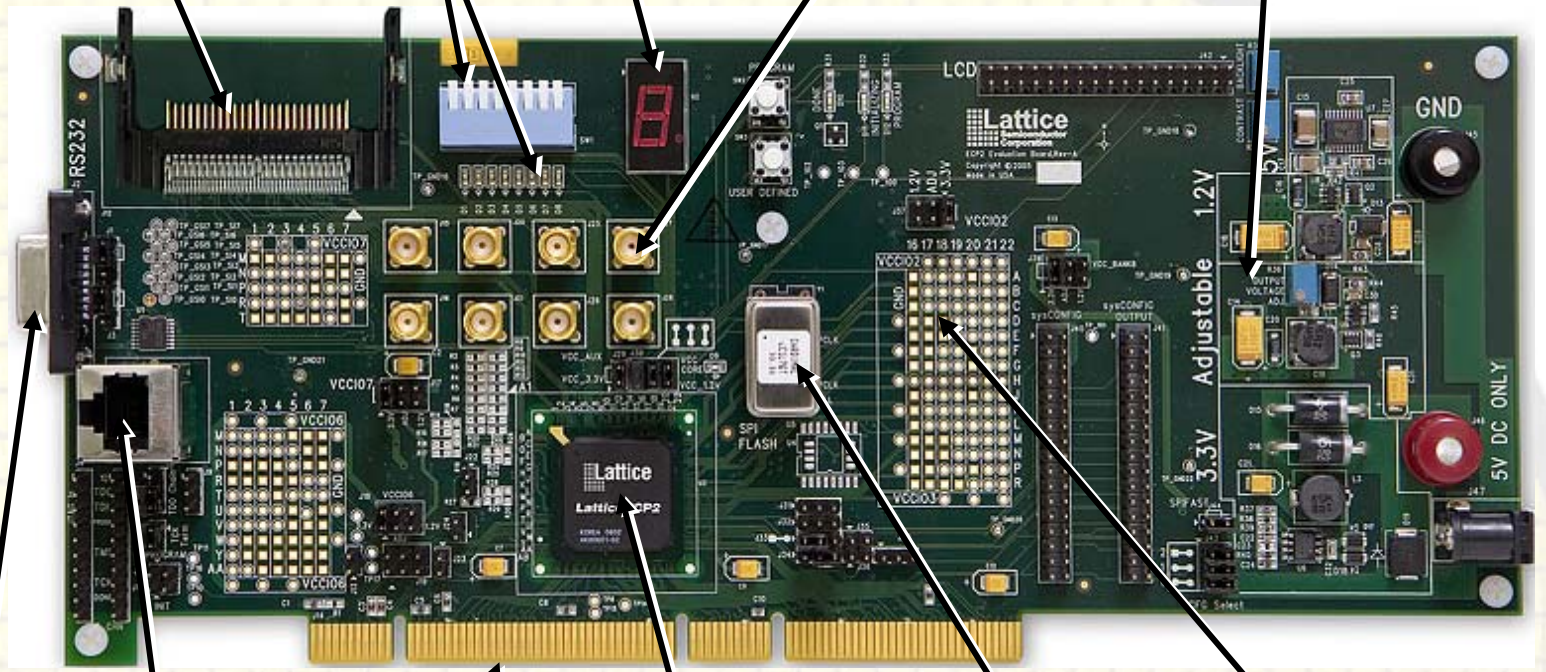
LatticeECP2 Standard Evaluation Board

- **Features:**
  - 64-bit PCI/PCI-x edge connector and form factor
  - RS-232 & RJ-45 Connectors
  - Compact Flash Connector
  - On-board Flash configuration memory
  - Prototype area
  - Various LEDs, switches, connectors, headers, and on-board power supply
  - Includes: ispDOWNLOAD Cable for device programming
  - Includes: AC power supply (International wall plug-in)
- **484 fpBGA Device**
  - ECP2-50: LFE2-50E-6F484C
- **Availability**
  - Available Now
- **On the web**
  - User guide (including schematics), sample program.

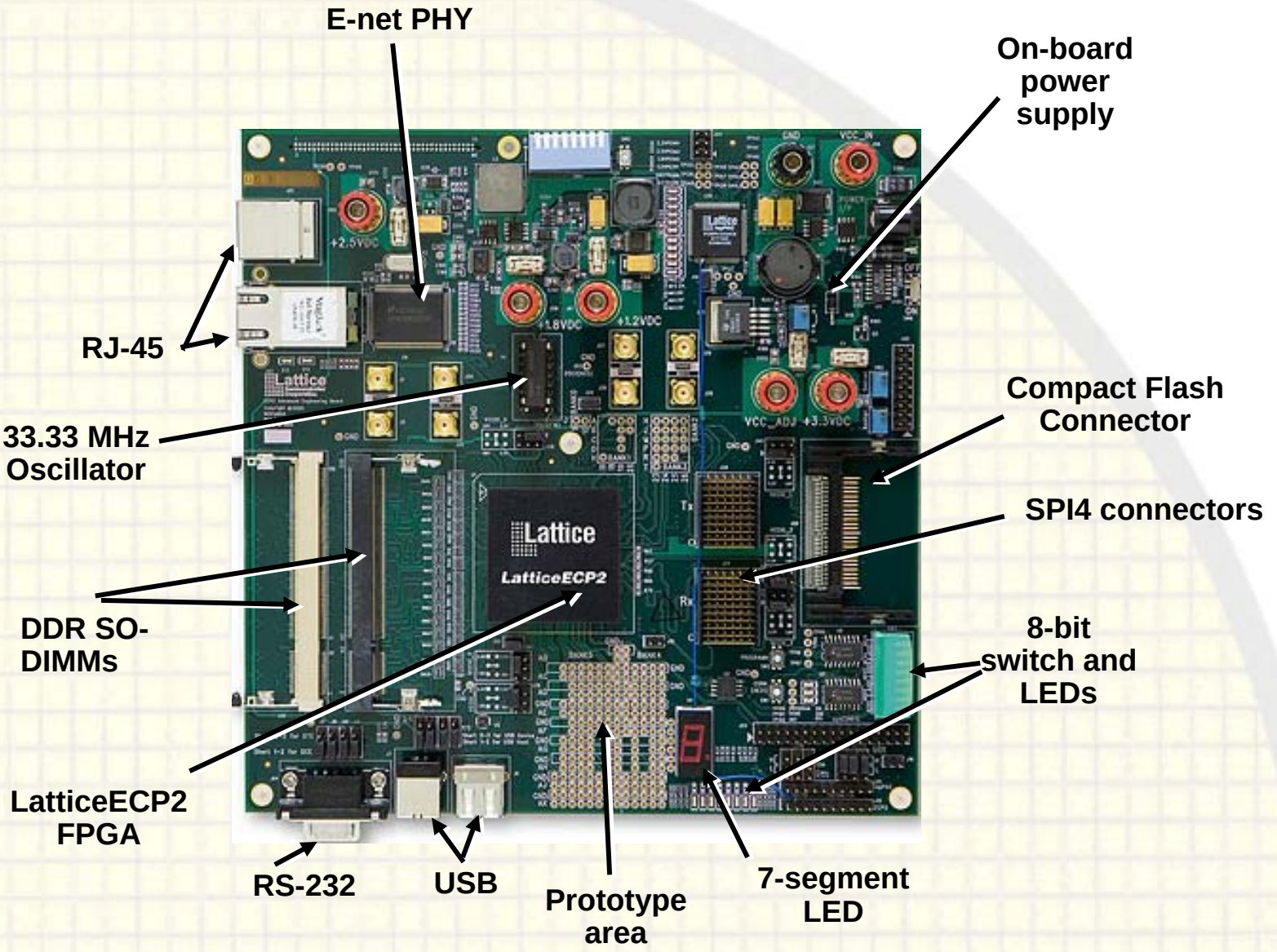
LatticeECP2 Standard Evaluation Board



LatticeECP2 Advanced Evaluation Board

- **Features:**
  - Dual DDR2 SO DIMM memory sockets
  - 10/100/1G Ethernet PHY with RJ-45 interface
  - SPI4.2 TX/Rx Connectors
  - RS232 Driver/Receiver
  - USB Transceiver
  - LCD panel interface
  - TI EMIF Interface Connector
  - On-board SPI-Flash configuration memory
  - Various LEDs, switches, connectors, headers, SMAs, on-board power supply, Lattice PAC-POWR1220AT8 Power Manager
- **672 ball device**
  - LFE2-50E-6F672C
- **Availability**
  - Available Now
- **On the web**
  - User guide (including schematics), sample program.

LatticeECP2 Advanced Evaluation Board



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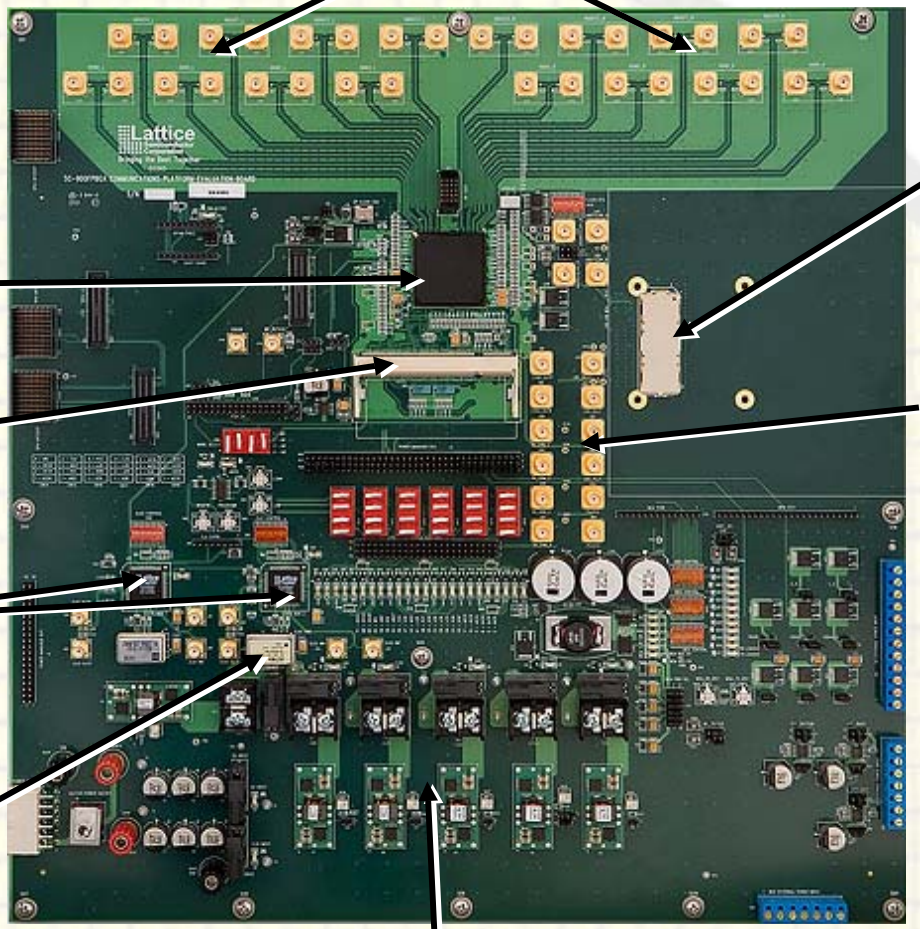
LatticeSC Communications Board

- **Features:**
  - 300-pin MSA transponder for SFI-4.1/XSBI applications
  - Molex VHDM interconnection for SPI4.2
  - 200-pin DDR SODIMM socket
  - SMA test points for high-speed SERDES (4 channels, 4 SMA each) and Clock I/O
  - On-board power control
  - On-board oscillator
  - On-board clock management
  - Various high-speed layout structures
  - On-board flash configuration memory
  - Various LEDs, switches, connectors, headers, etc.
- **900 ball device**
  - LatticeSC: LFSC3GA25E-6F900C
- **Availability**
  - Contact your Lattice Representative
- **On the web**
  - User Guide and general info

LatticeSC Communications Board



LatticeSC Standard Board

- **Features:**
  - X8 PCIexpress edge connector / form factor
  - On-board DDR2 Memory
  - SMA Connectors for SERDES I/O, LVDS evaluation, and external clock I/O
  - BNC edge connectors for Digital Video Interface
  - On-board Flash configuration memory
  - Various LEDs, switches, connectors, headers, and on-board power control
- **1152 ball device**
  - LatticeSC: LFSC3GA80E-6FF1152C
- **Availability**
  - 3Q 2006
- **On the web**
  - Related info coming soon!

LatticeEC Standard Evaluation Board

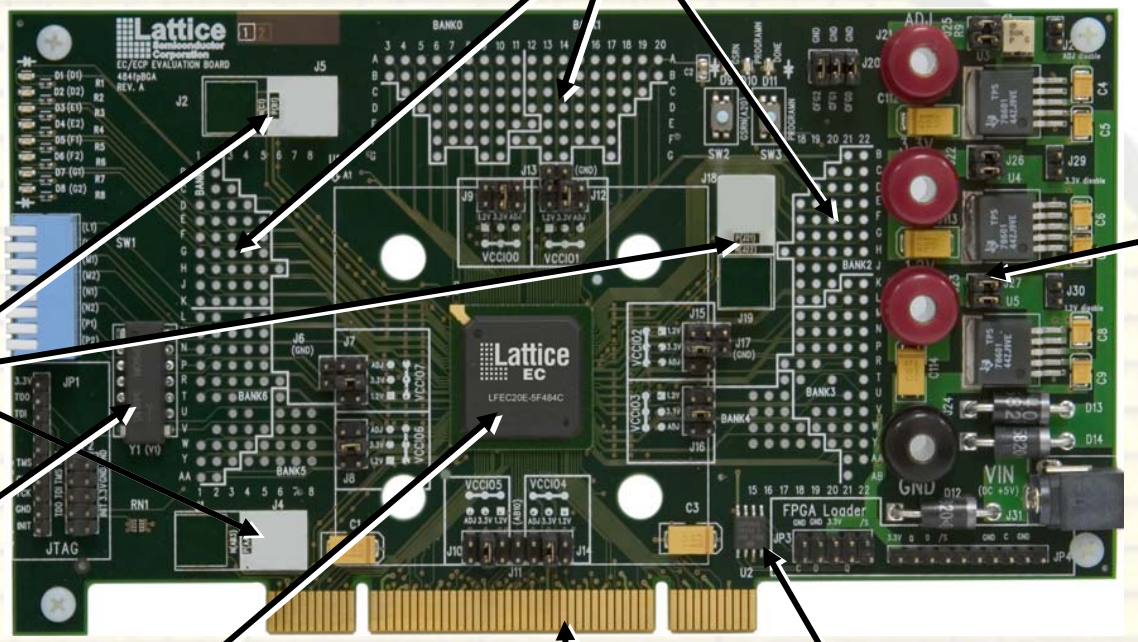
- **Features:**
  - PCI connector
  - oscillator socket / ext clock
  - 1.2V & 3.3V on-board power (banana jacks also available)
  - SPI flash on-board
  - Pads for high-speed SMA connectors (not populated)

- **484-ball device**
  - EC6: LFEC6E-L-EV – List Price = $149
  - EC20: LFEC20E-L-EV – List Price = $175
  - ECP20: LFECP20E-L-EV – List Price = $175

- **Availability:**
  - Available Now

- **On the web**
  - PCI evaluation bitstream available
  - Note there are both Rev A and Rev B PCBs = each has unique user manual/schematics

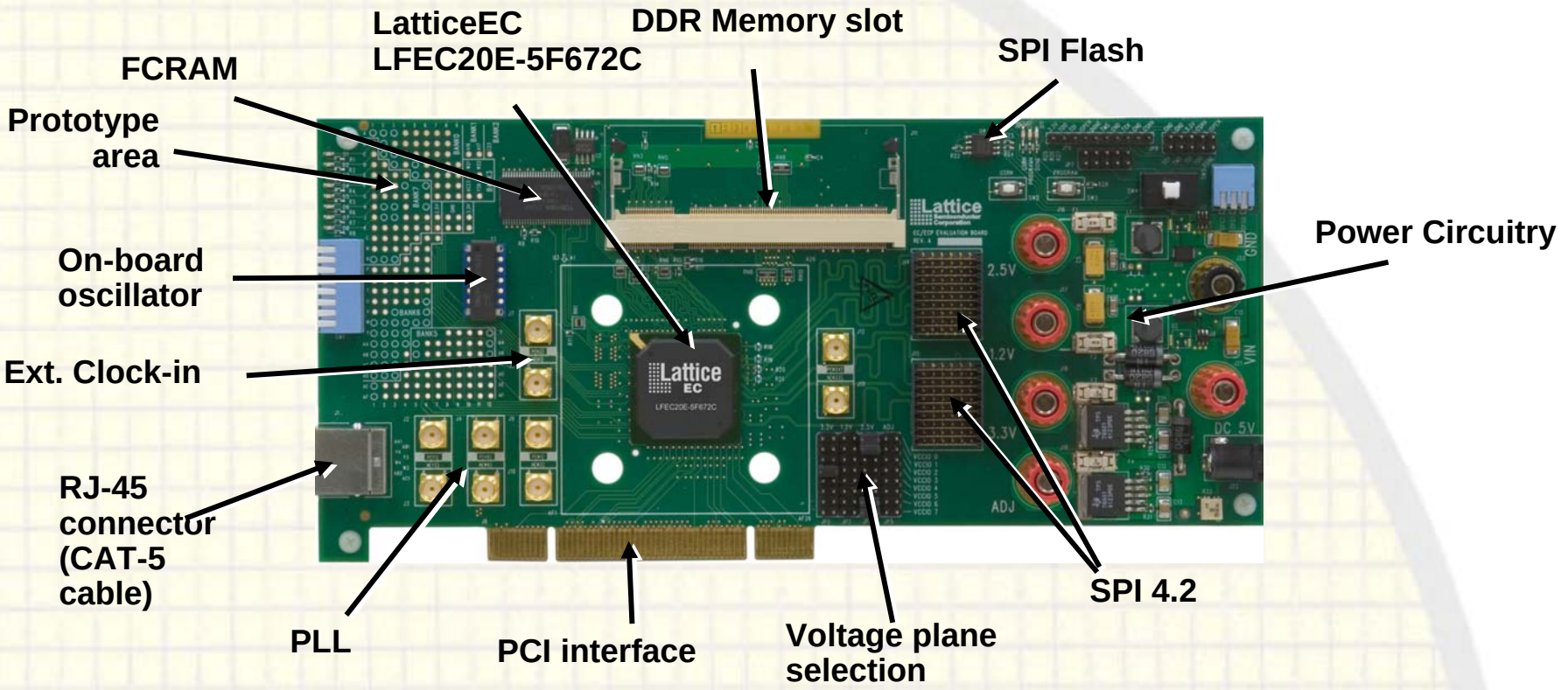
LatticeEC Standard Evaluation Board



LatticeEC Advanced Evaluation Board

- **Features:**
  - FCRAM on-board
  - DDR socket
  - SPI4.2 interface
  - RJ-45 interface
  - PCI slot
  - Multiple voltage planes
  - SPI Flash on-board
  - SMA connectors for high-speed signals / clocks
  - On-board/ext clock, etc.
- **672-ball device**
  - EC20: LFEC20E-H-EV – List Price = $1295
  - ECP20: LFECP20E-H-EV – List Price = $1295
- **Availability**
  - Contact your Lattice Representative
- **On the web**
  - PCI evaluation bitstream available
  - FCRAM evaluation bitstream available
  - DDR evaluation bitstream available
  - User manual w/ schematics

LatticeEC Advanced Evaluation Board



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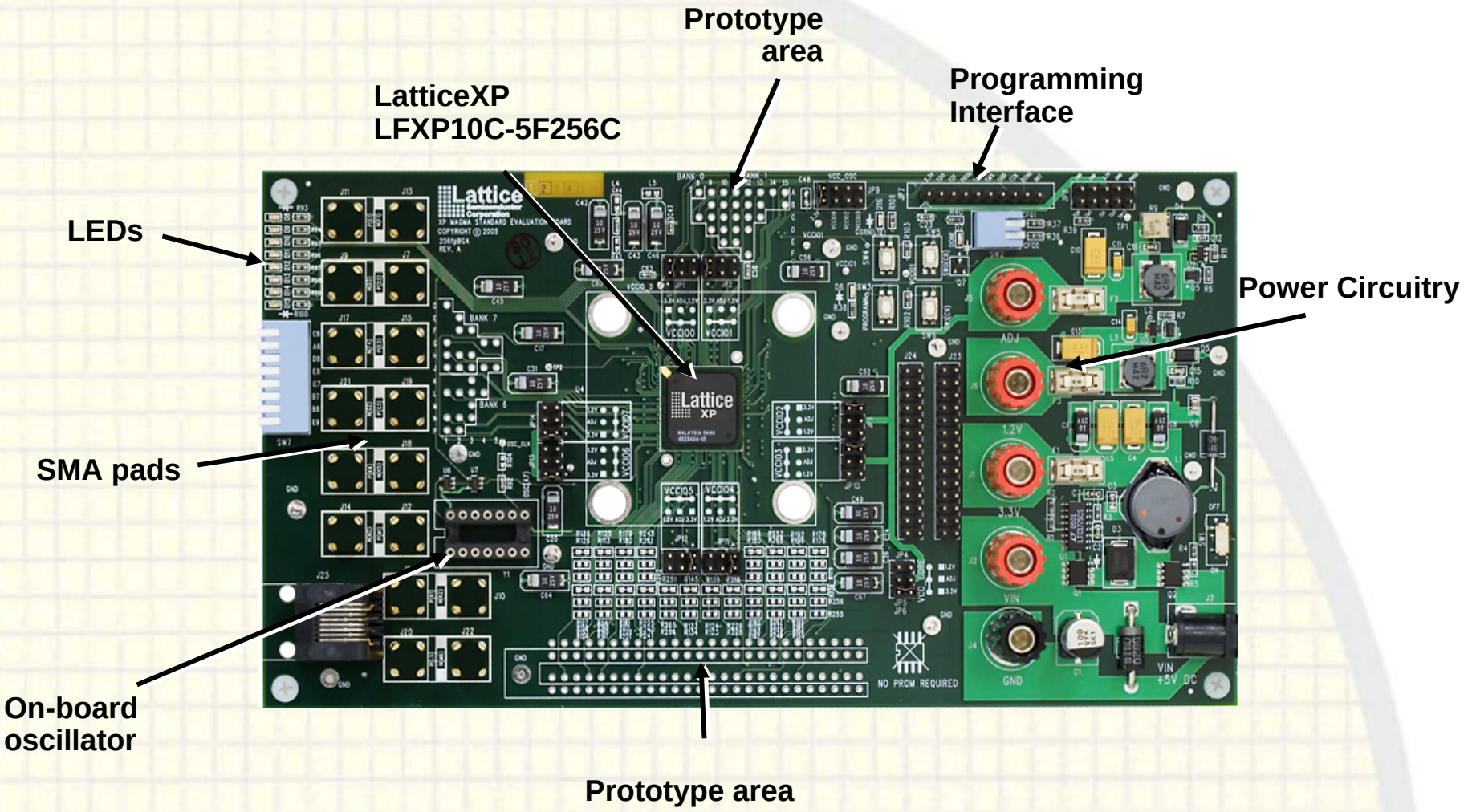
LatticeXP Standard Evaluation Board

- **Features:**
  - Multiple power planes (external sources available)
  - On board oscillator
  - SMA pads for high-speed signaling (SMA pads not populated)
  - LEDs & switches for feedback & configuration
  - Generous prototype area
  - On-board power supply (Note: Initial Rev. A boards did not include this)
- **256-ball device**
  - XP10: LFXP10C-L-EV
- **Availability**
  - Rev B boards now including AC adapter and download cable.
- **On the web**
  - User manual, sample program.

LatticeXP Standard Evaluation Board



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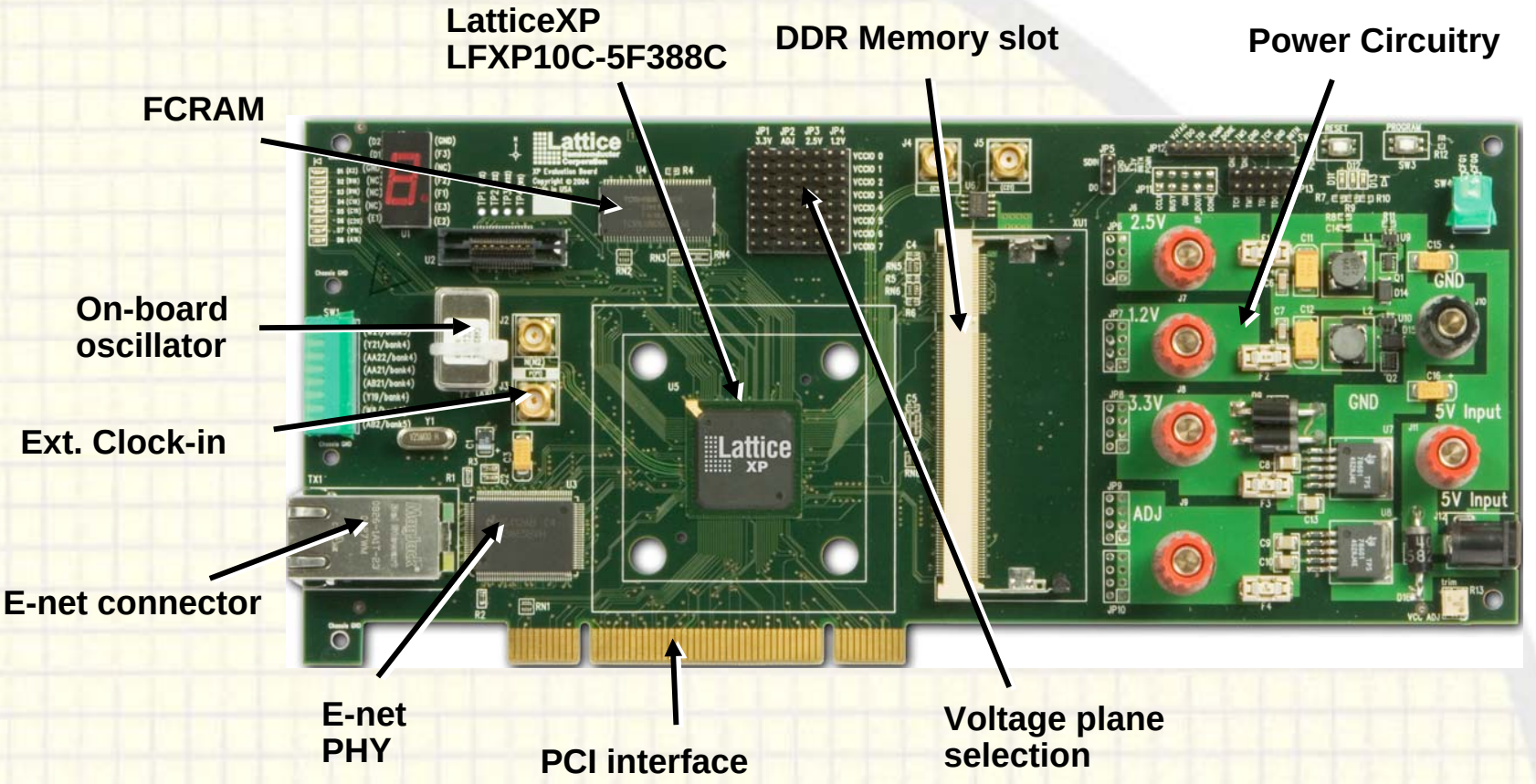
LatticeXP Advanced Evaluation Board

- **Features:**
  - LFXP10C-5F388C FPGA Device
  - DDR memory interface socket
  - 10/100/1G E-net MAC interface
  - PCI interface
  - On-board FCRAM
  - On-board oscillator
  - Various LEDs, SMA connections for external clocking, and on-board power control
- **388-ball device**
  - XP10: LFXP10C-H-EV – List Price = $1295
- **Availability**
  - Contact your Lattice Representative
- **On the web**
  - Evaluation bitstreams when available
  - User manual w/ schematics when available

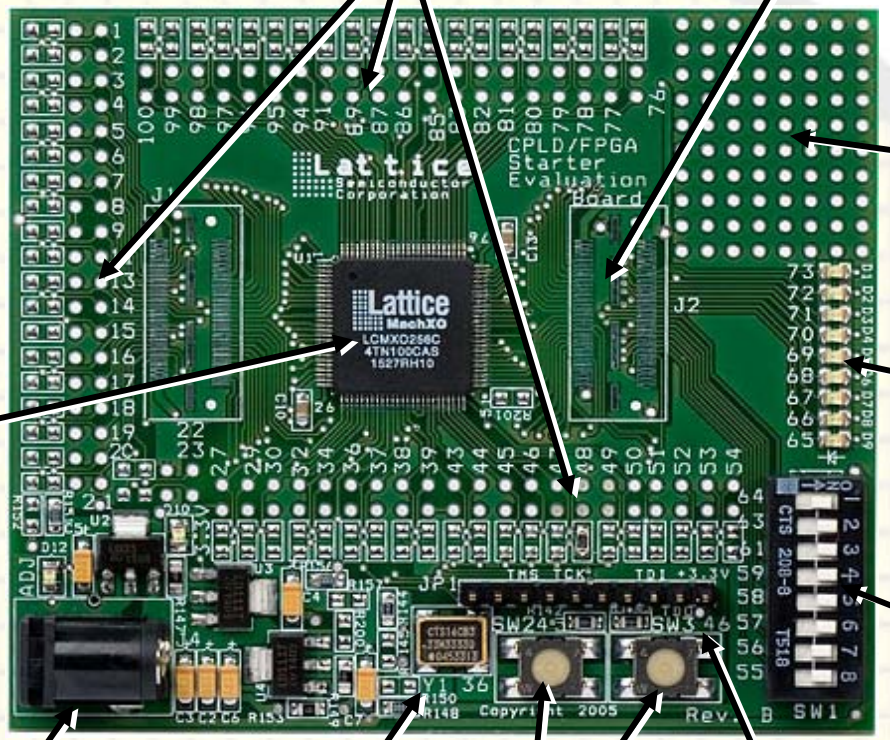
LatticeXP Advanced Evaluation Board



MachXO Starter Evaluation Board

- **Features**
  - MachXO device
  - Power input jack
  - 33MHz oscillator
  - Status LEDs, and 9 I/O LEDs
  - 8-bit input switch
  - Access to all device I/O
  - Prototyping area
  - Landing pads for off-board expansion connectors
  - AC adapter Included (International plugs!)
  - Download Cable Included: HW-DL-3C
- **100-TQFP device**
  - MachXO-256: LCMXO256C-4T100C
- **Availability**
  - Shipping today, order via on-line store, or through your Distributor
  - Board + AC Adapter + Download Cable = $99, An incredible value!
- **On the web**
  - User Manual available for download, includes schematics.

MachXO Starter Evaluation Board



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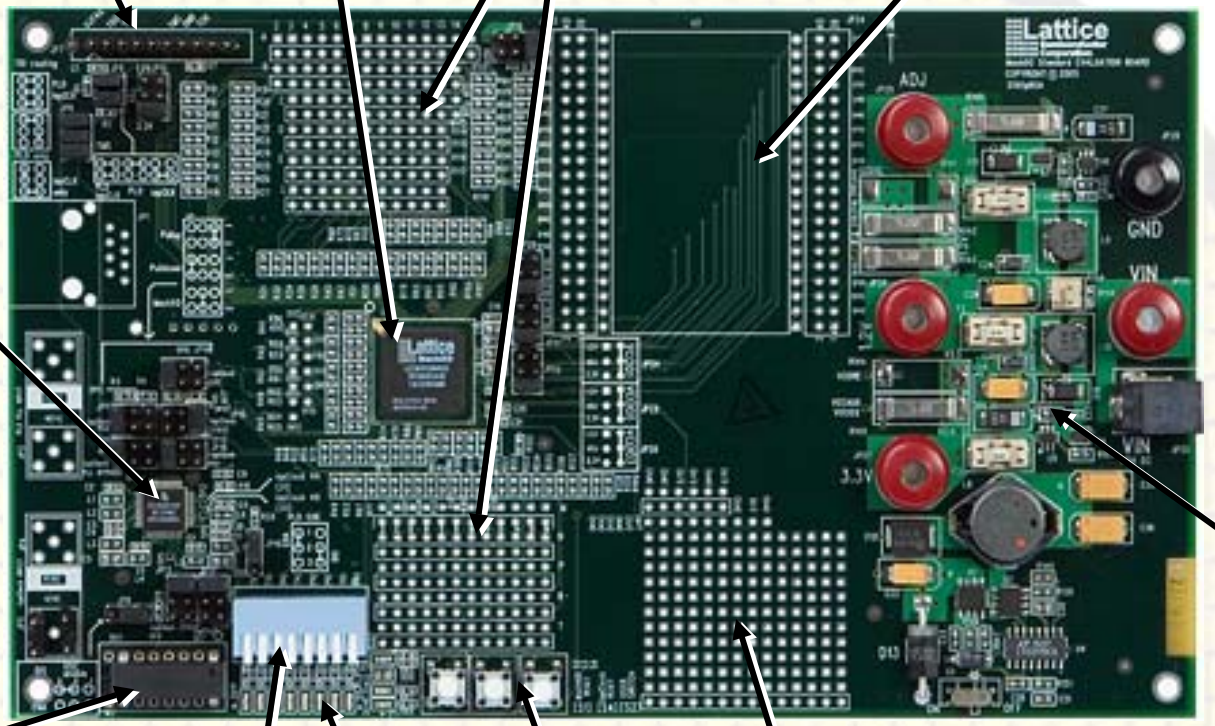
MachXO Standard Evaluation Board

- **Features**
  - MachXO device
  - Power input jack
  - 3.3V, 1.2V and adjustable power planes
  - Adjustable oscillator
  - Lattice ispClock5610 Clock Manager: ispPAC-CLK5610V-01T48C
  - Status LEDs, and 8 I/O LEDs
  - 8-bit input switch
  - Access to all device I/O
  - Prototyping area
  - Landing pads for LCD display
  - AC Adapter included
- **256-BGA device**
  - MachXO-640: LCMXO640C-4F256C
  - MachXO-2280: LCMXO2280C-4F256C
- **Availability**
  - MachXO-640 version: Available Now
  - MachXO-2280 version: Available Now
- **On the web**
  - User Manual and sample program

MachXO Standard Evaluation Board



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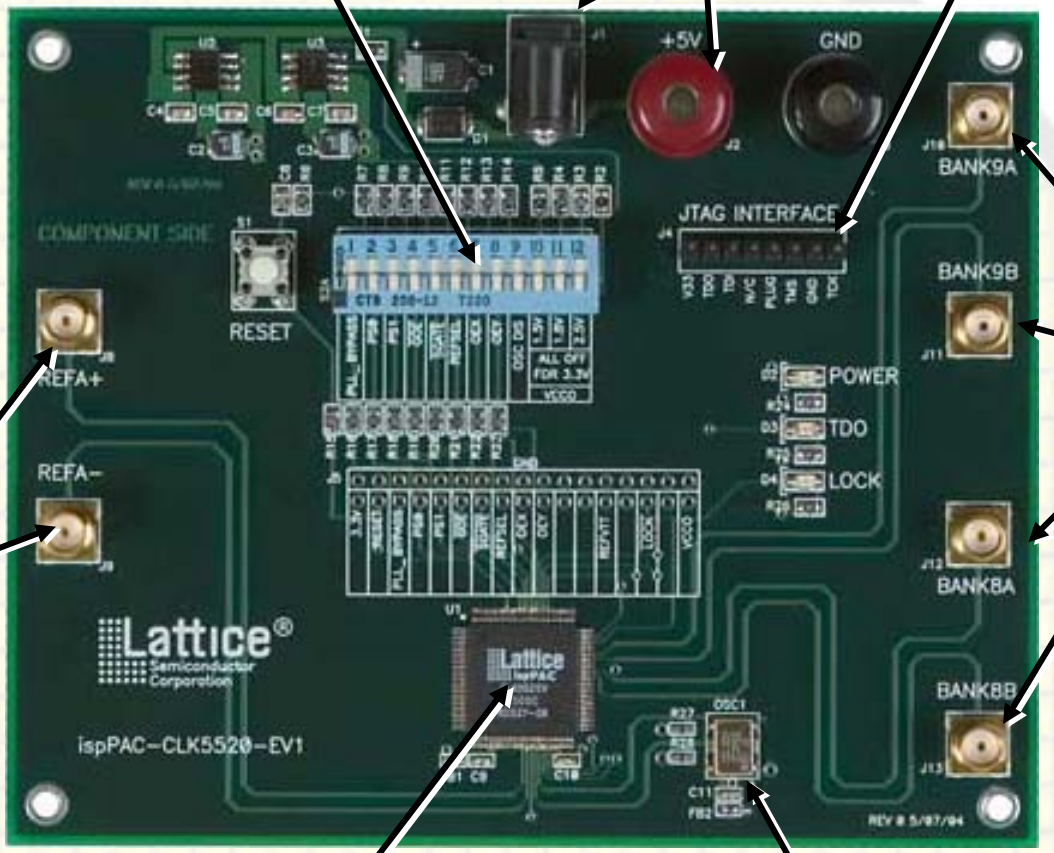
PAC – CLK5620 Evaluation Board

- **Features:**
  - General purpose header for user I/O
  - SMA connectors to selected high-speed I/O signals
  - LEDs for status indication,
  - Switches for added flexibility
  - JTAG interface
- **100-TQFP device**
  - ispPAC-CLK5620V-01T100C (20 outputs, 100-pin TQFP package)
  - Board Only: PACCLK5620-EV – List Price = $225
  - Development Kit: PAC-SYSTEMCLK5620 – List Price = $295
    - » Kit Includes PAC-Designer software & Download cable.
- **Availability**
  - Available now
- **On the web**
  - Applications note including schematics
  - PAC-Designer Software

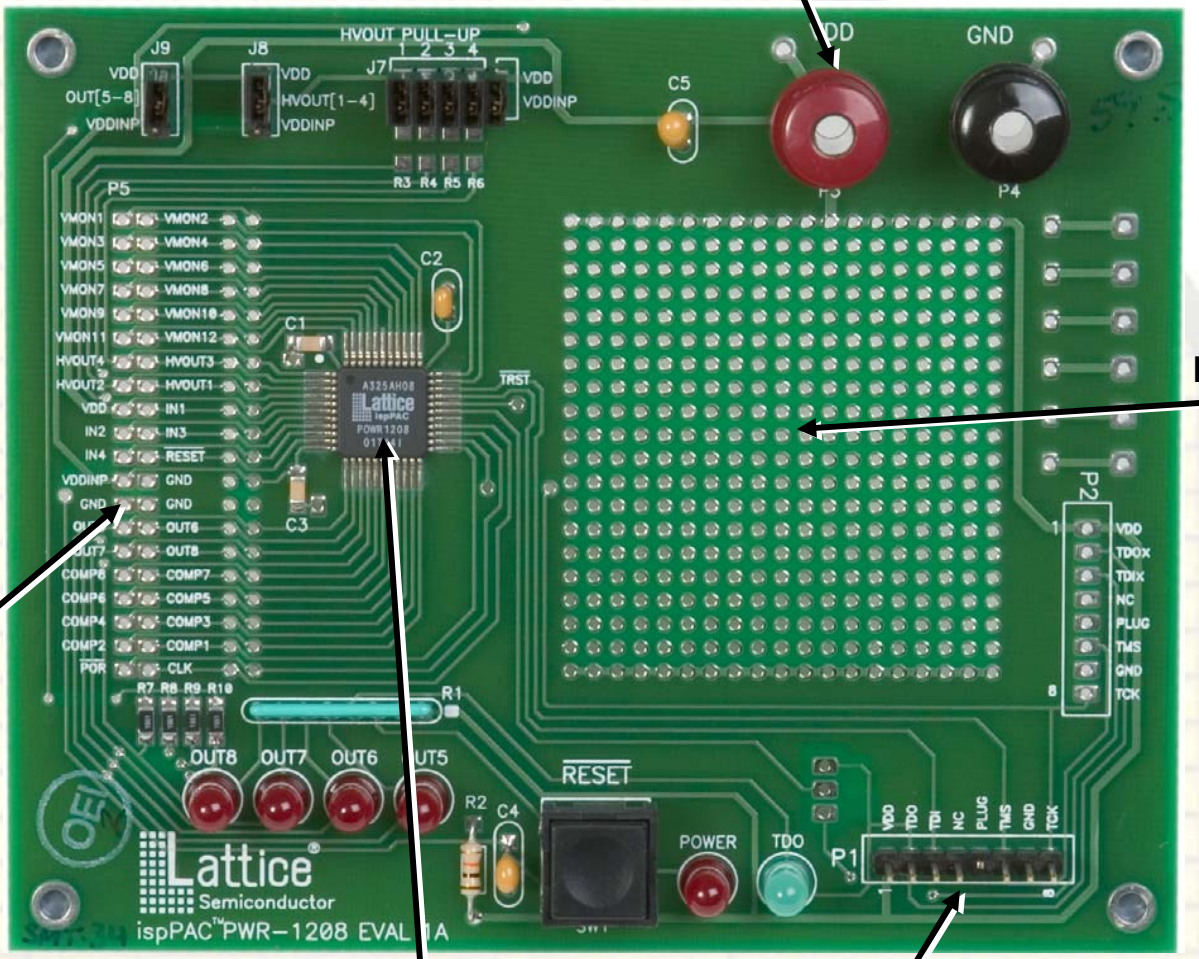
PAC – CLK5620 Evaluation Board



PAC – POWR1208/P1 Evaluation boards

- **Features:**
  - Large prototype area
  - Access to all device I/O
  - LEDs for status indication
  - JTAG interface
- **100-TQFP device**
  - ispPAC-POWR1208 (44-pin TQFP package) (also available with 1208P1)
  - Board Only: PACPOWR1208-EV – List Price = $99
  - Development Kit: PAC-SYSTEMPOWR1208 – List Price = $125
    - » Kit Includes PAC-Designer software & Download cable.
- **Availability**
  - 1208 and 1208P1 boards Available now
- **On the web**
  - Applications note including schematics
  - PAC-Designer Software

PAC-POWR1208/P1 Evaluation Board



Programming Hardware / Cables

- Parallel and USB Compatible Programming Cables
- Model 300 Desktop Programmers
- Programming Adapters

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Agenda

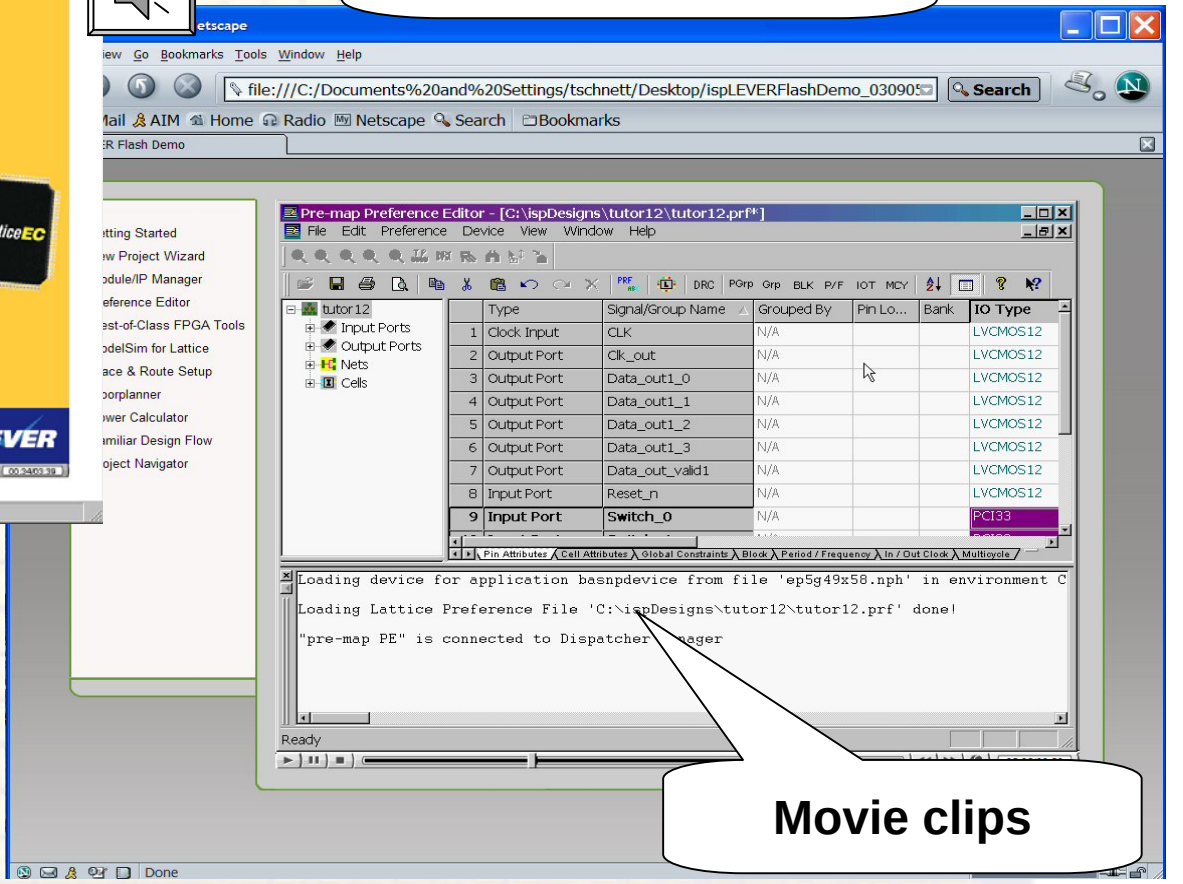
- ispLEVER Software Feature Overview
- ispLEVER Versus the Competition
- ispLeverCORE Overview
- PAC-Designer Software Feature Overview
- Development Hardware
- How to Learn More

Web Site Content

ispLEVER Flash Demo

- **Self-Running Narrative and Demo Movies**
  - **Updated each release**
  - **Getting Started, Best-of-Class Tools, and a Familiar Design Flow**

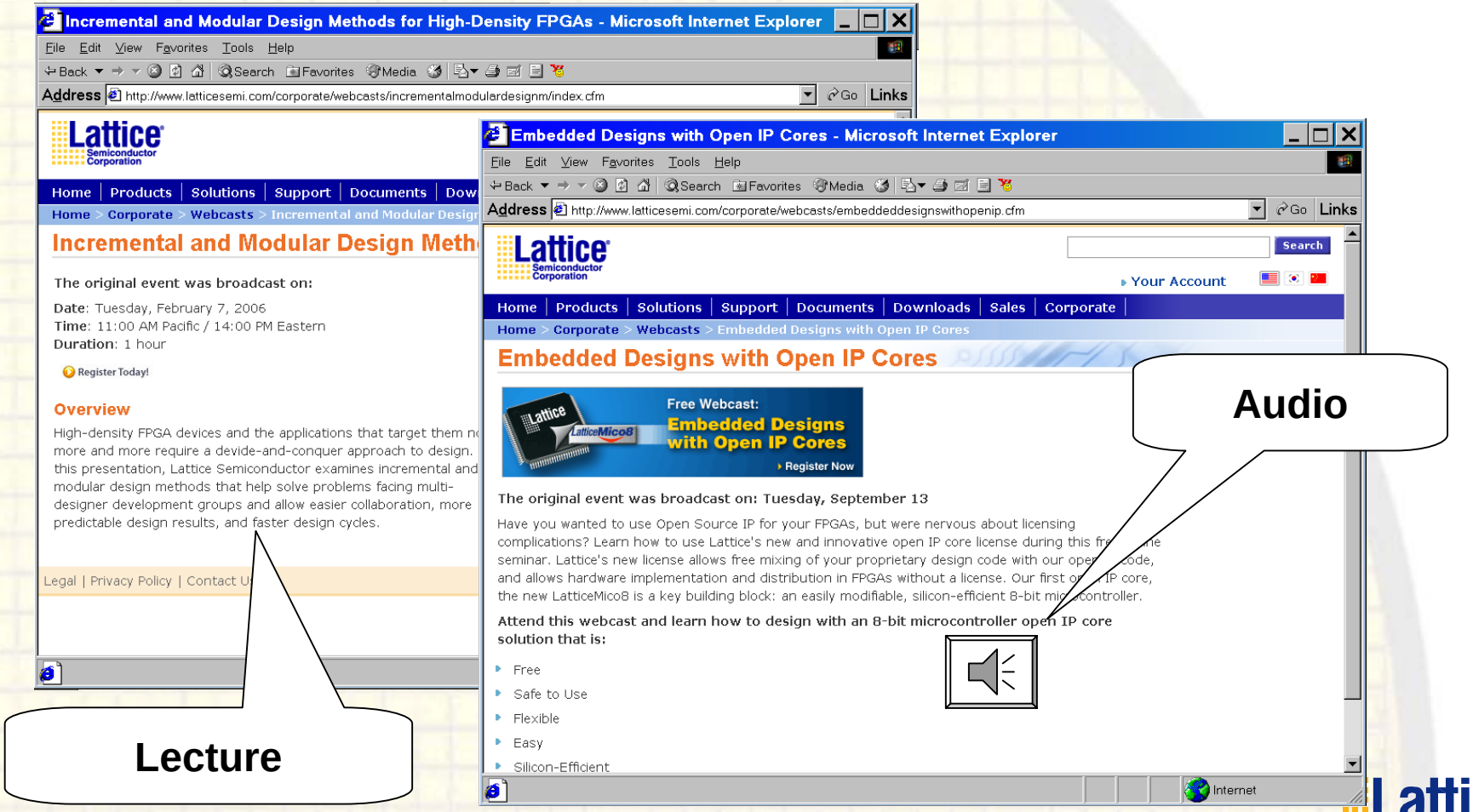
Audio



Movie clips

On-Demand Webcasts

- Software and IP Design Methods and Techniques
- Attend Live Broadcasts and Interact with Presenter
- Hear Archives Anytime



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Conclusion

- Complete Solutions for All Your Needs
- Powerful / Full Featured Solutions
- Easy to Learn and Use
- Only Lattice's ispLEVER Design Tools Offer:
  - Leading 3rd party tools
  - Performance leadership
  - The best software prices and value
- PAC-Designer Mixed Signal Design Solutions
- A Complete Library of ispLeverCORE IP
- Complete Programming Hardware & Software
- Evaluation Boards For
  - FPGA / FPSC
  - CPLD
  - Mixed Signal Devices